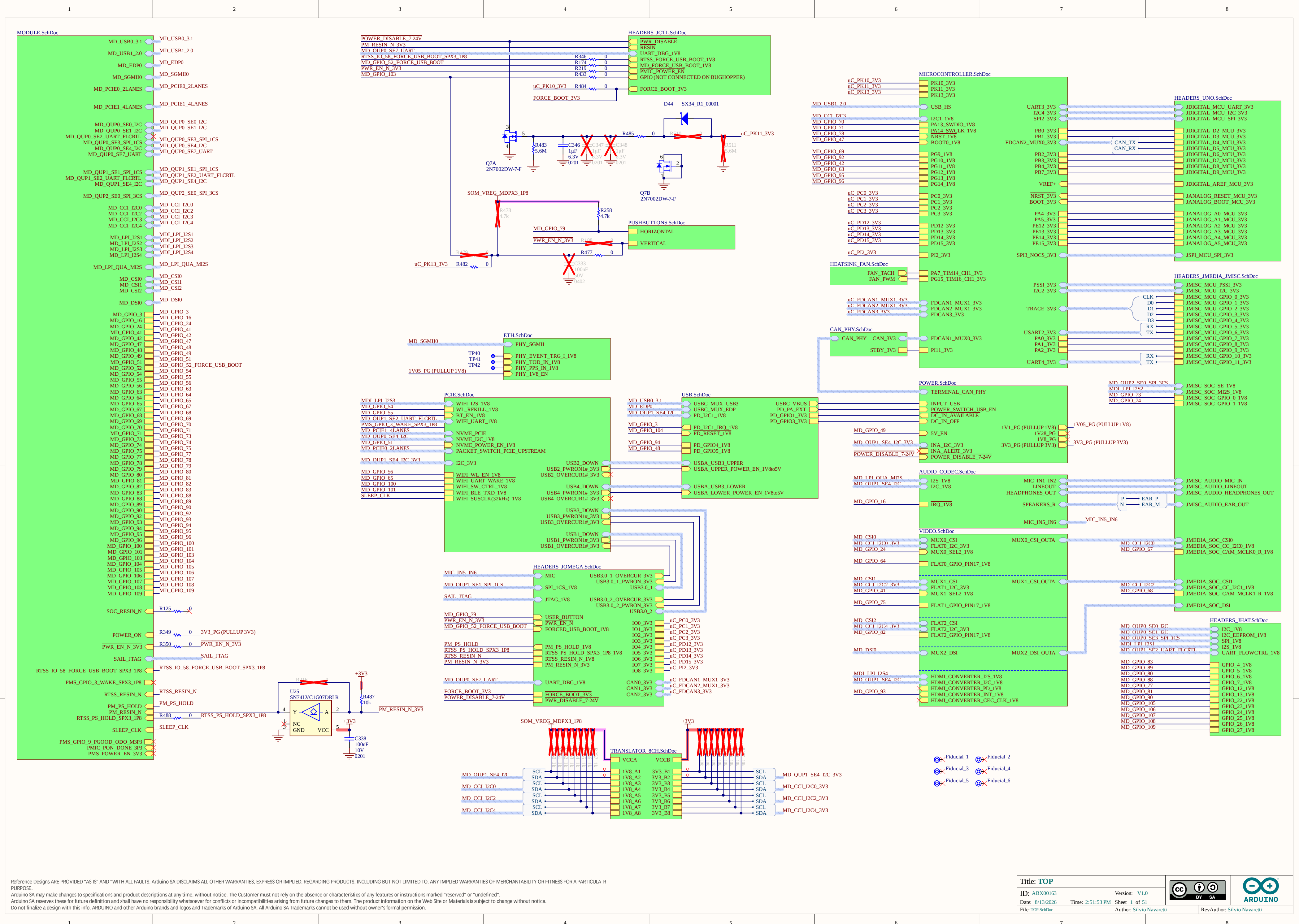
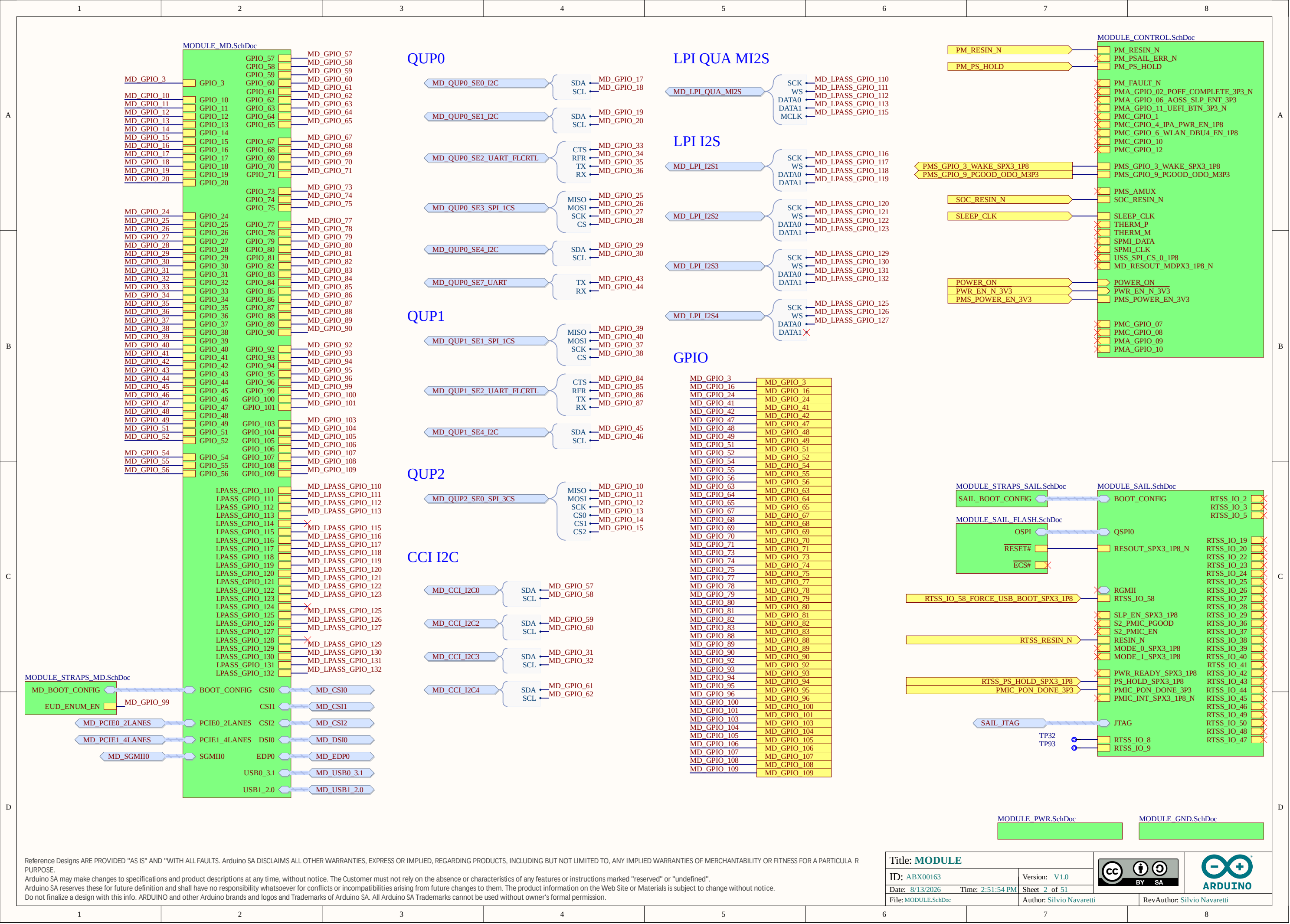






A

A

B

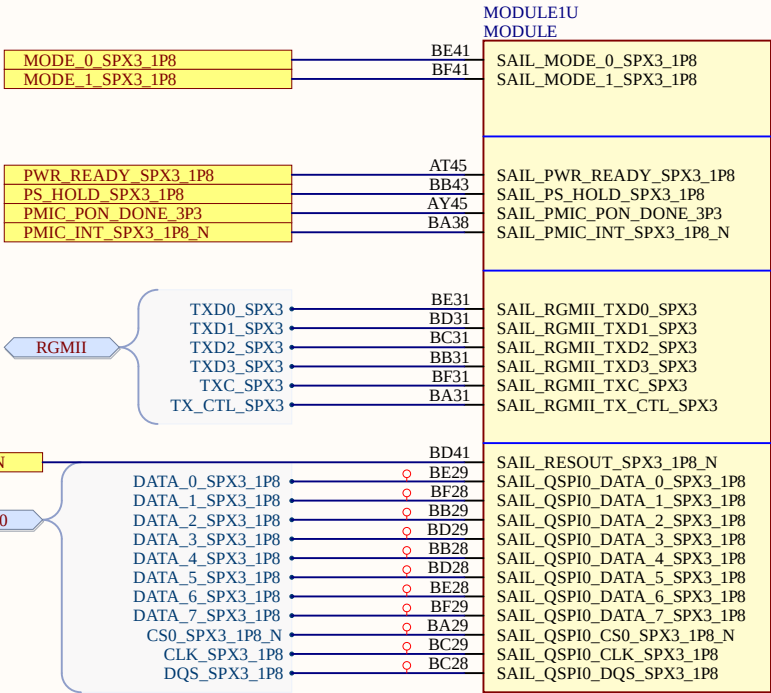
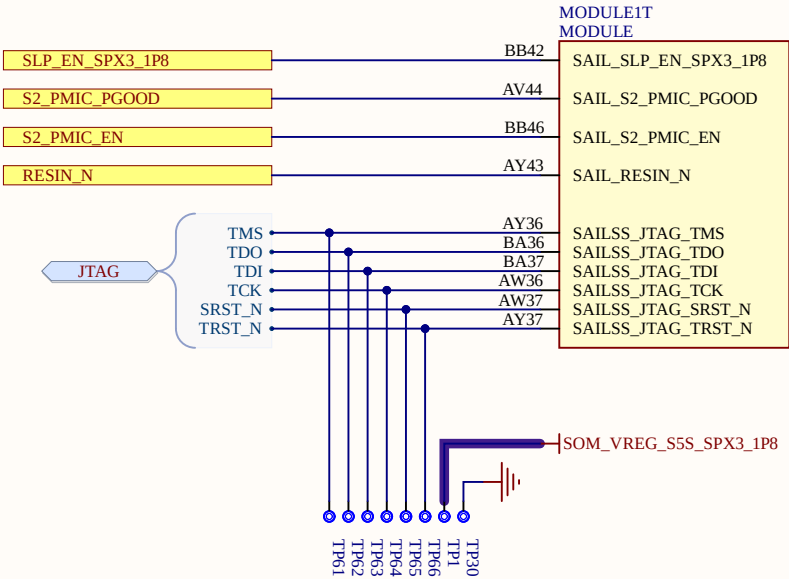
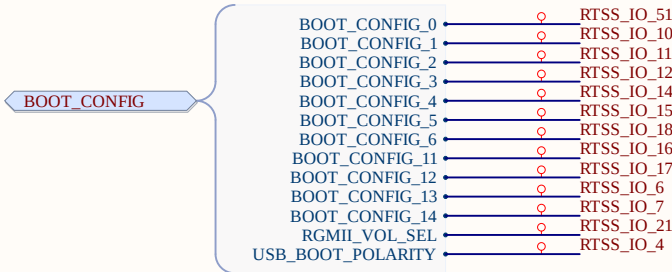
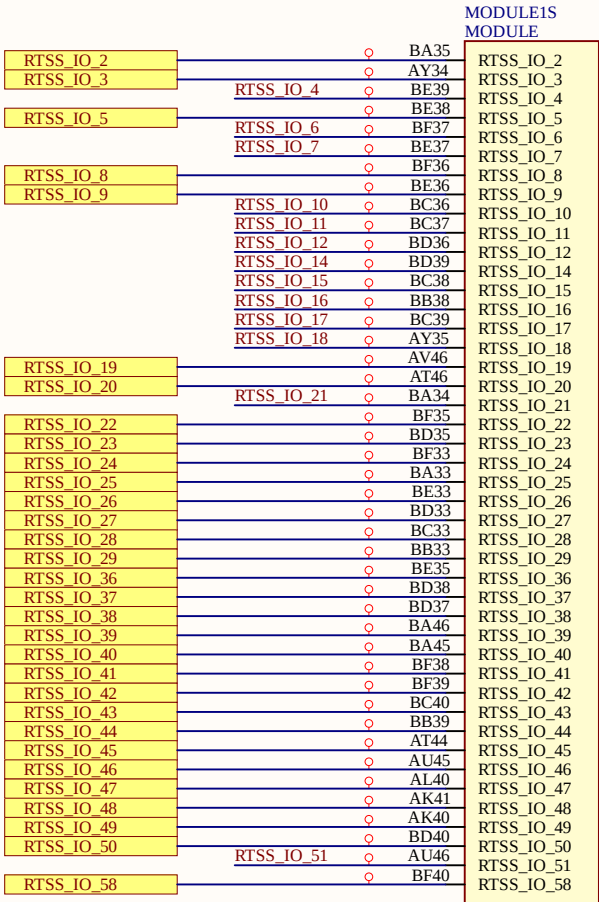
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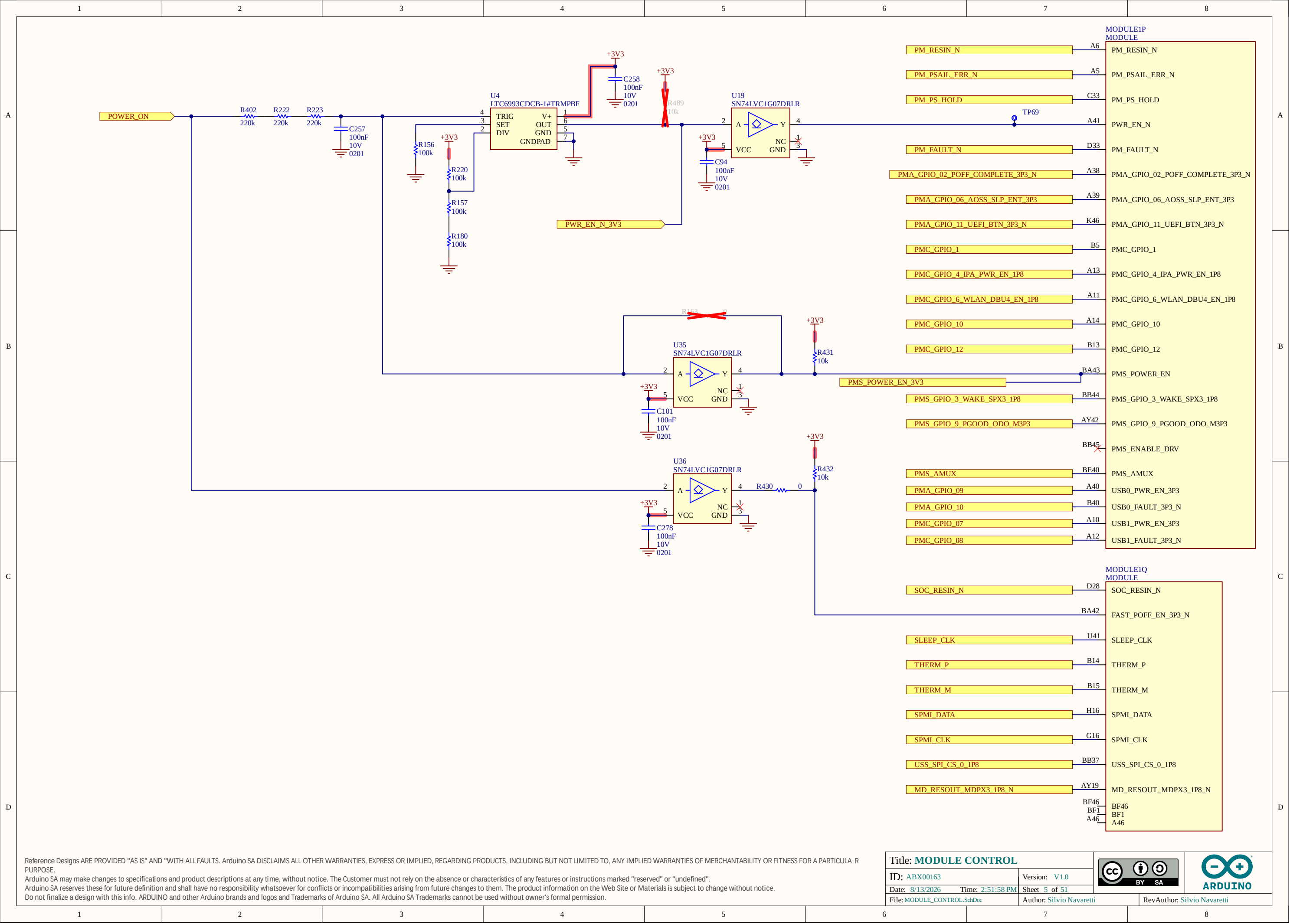
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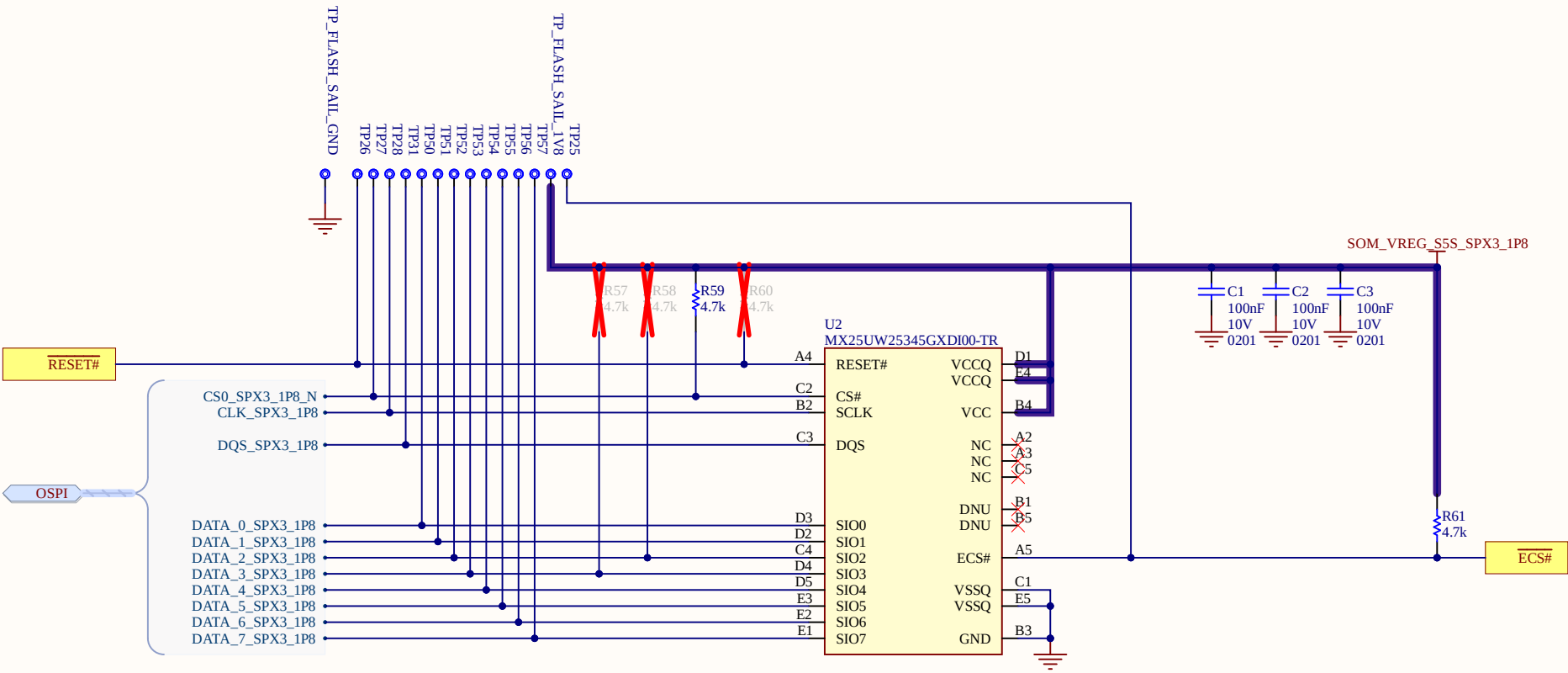
C

D

D







RESET#

OSPI

CS0_SPX3_1P8_N
CLK_SPX3_1P8
DQS_SPX3_1P8

DATA_0_SPX3_1P8
DATA_1_SPX3_1P8
DATA_2_SPX3_1P8
DATA_3_SPX3_1P8
DATA_4_SPX3_1P8
DATA_5_SPX3_1P8
DATA_6_SPX3_1P8
DATA_7_SPX3_1P8

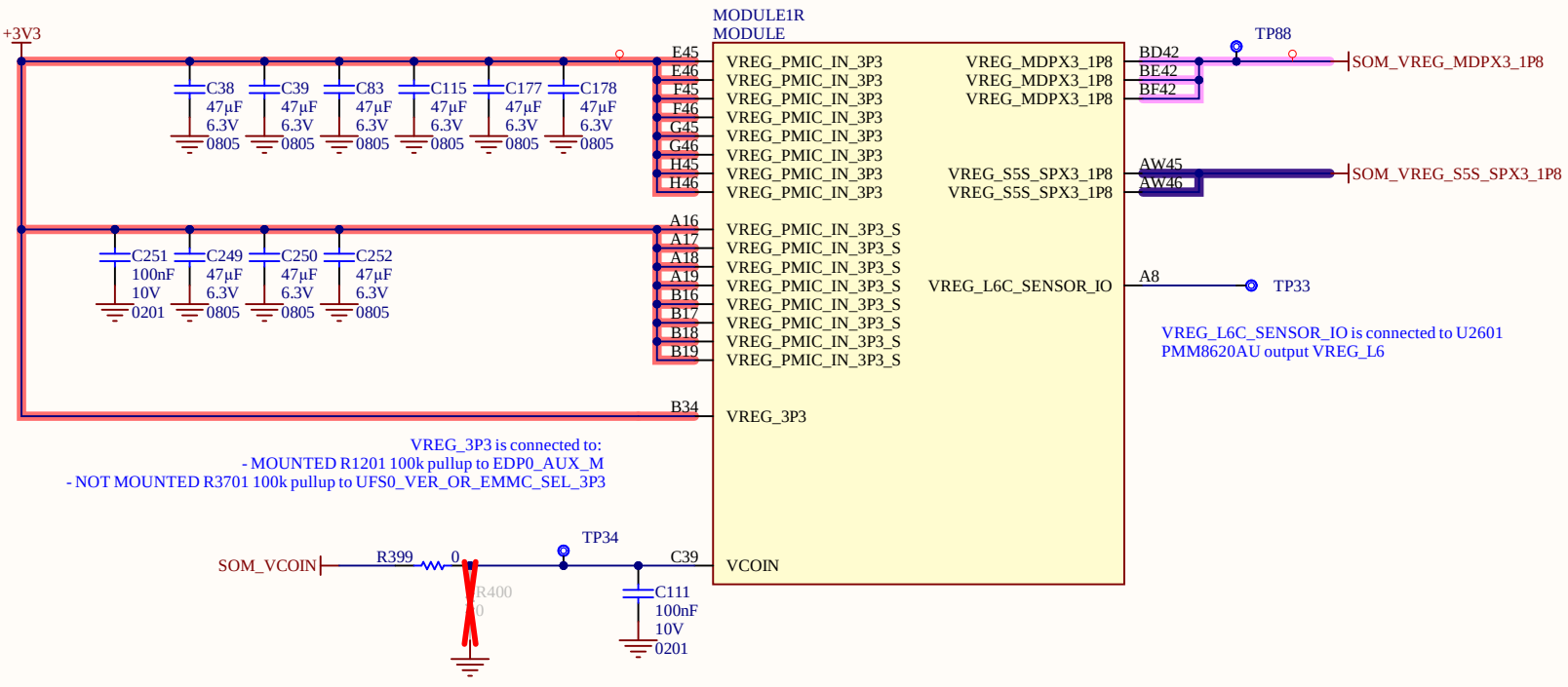
U2
MX25UW25345GXD100-TR
RESET#
CS#
SCLK
DQS
SIO0
SIO1
SIO2
SIO3
SIO4
SIO5
SIO6
SIO7
VCCQ
VCCQ
VCC
NC
NC
NC
DNU
DNU
ECS#
VSSQ
VSSQ
GND

SOM_VREG_S5S_SPX3_1P8

C1
100nF
10V
0201
C2
100nF
10V
0201
C3
100nF
10V
0201

ECS#

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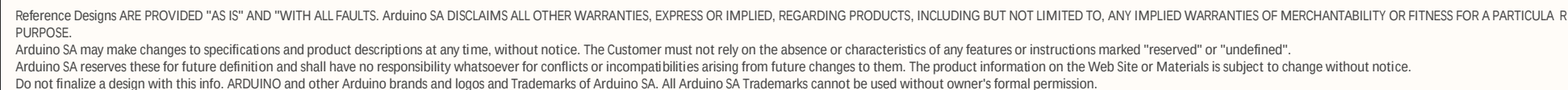
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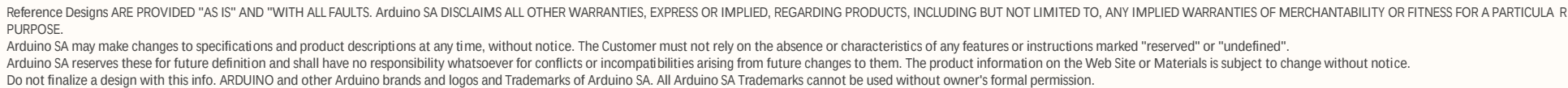
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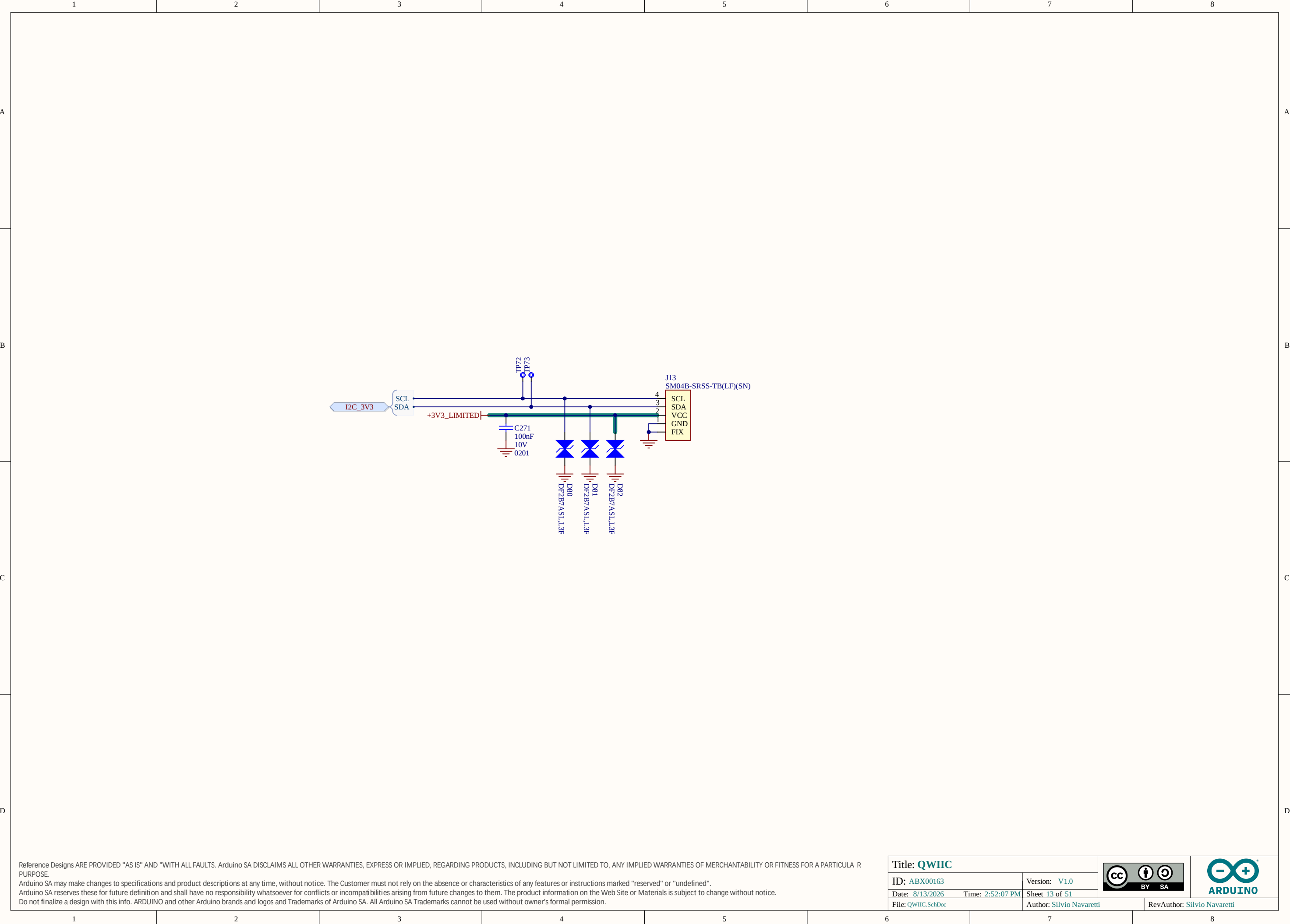
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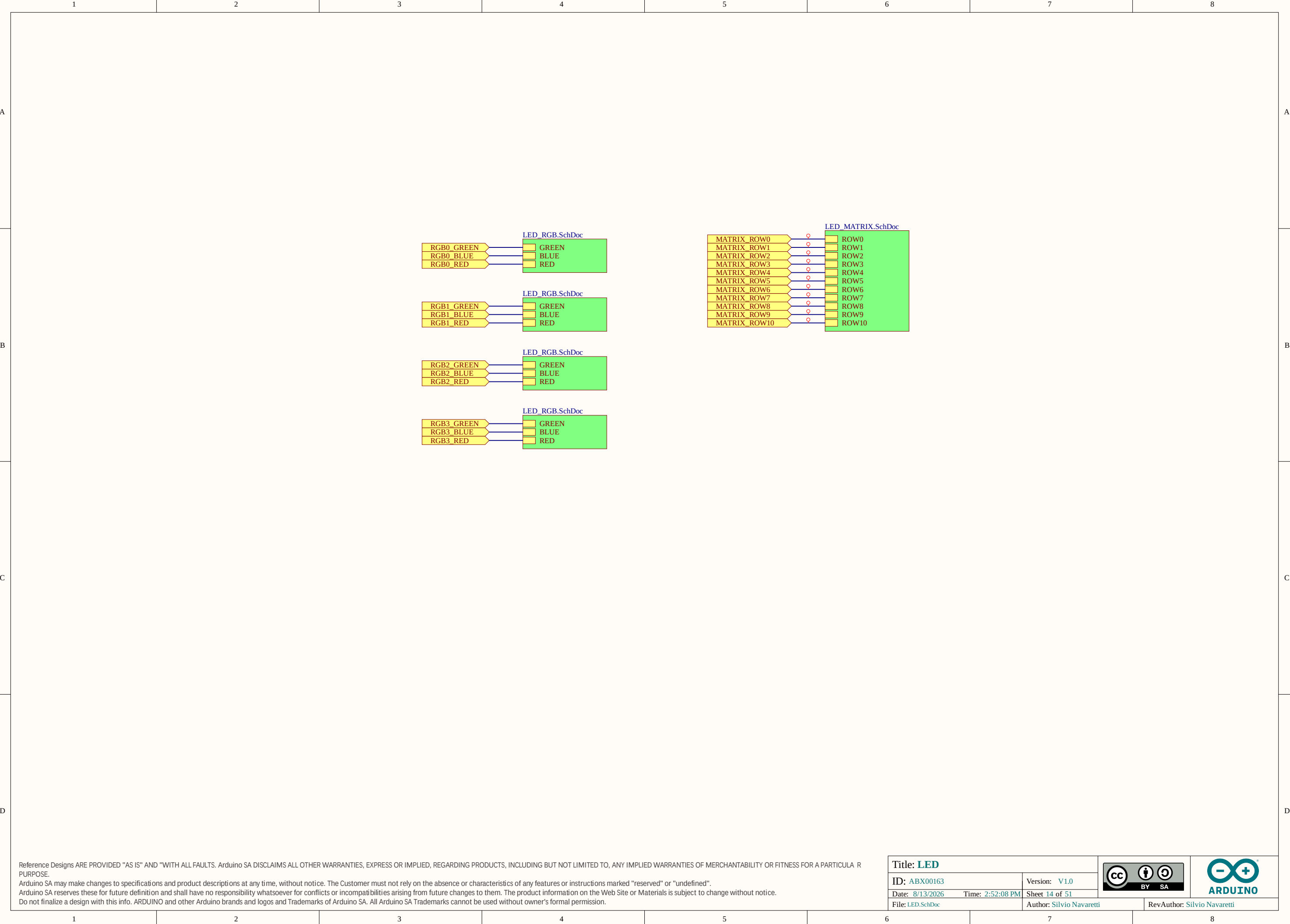


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Title: LED

ID: ABX00163

Date: 8/13/2026

File: LED.SchDoc

Version: V1.0

Time: 2:52:08 PM

Author: Silvio Navaretti

Sheet 14 of 51

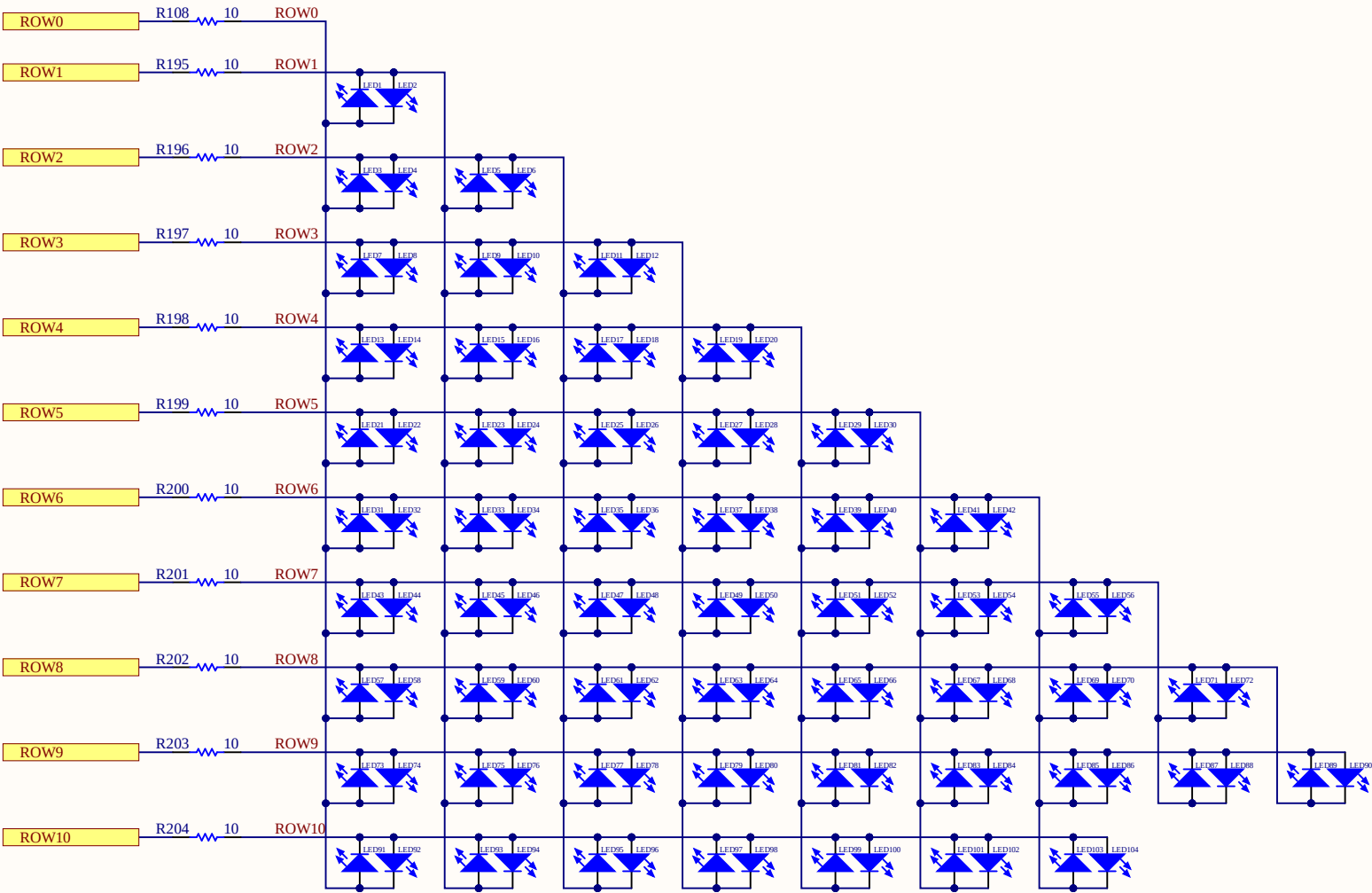
RevAuthor: Silvio Navaretti

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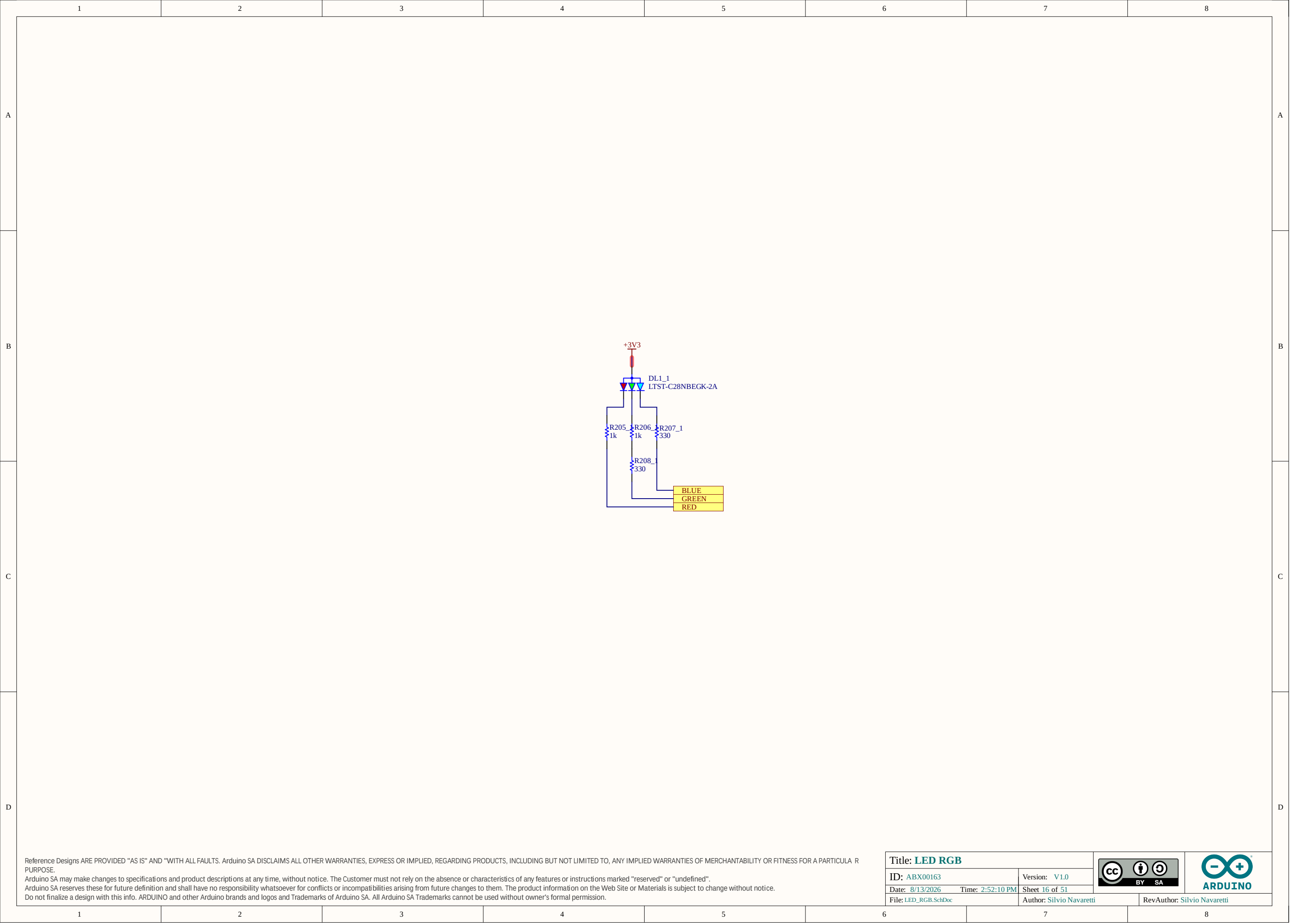
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Title: LED MATRIX				
ID: ABX00163	Version: V1.0			
Date: 8/13/2026	Time: 2:52:09 PM	Sheet 15 of 51	Author: Silvio Navaretti	RevAuthor: Silvio Navaretti
File: LED_MATRIX.SchDoc				



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A

A

B

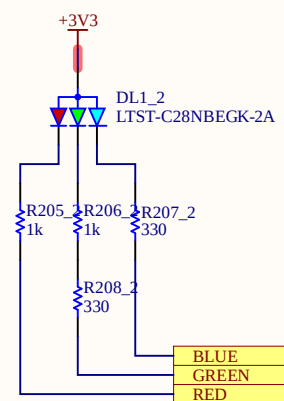
B

C

C

D

D



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Title: LED RGB

ID: ABX00163

Version: V1.0

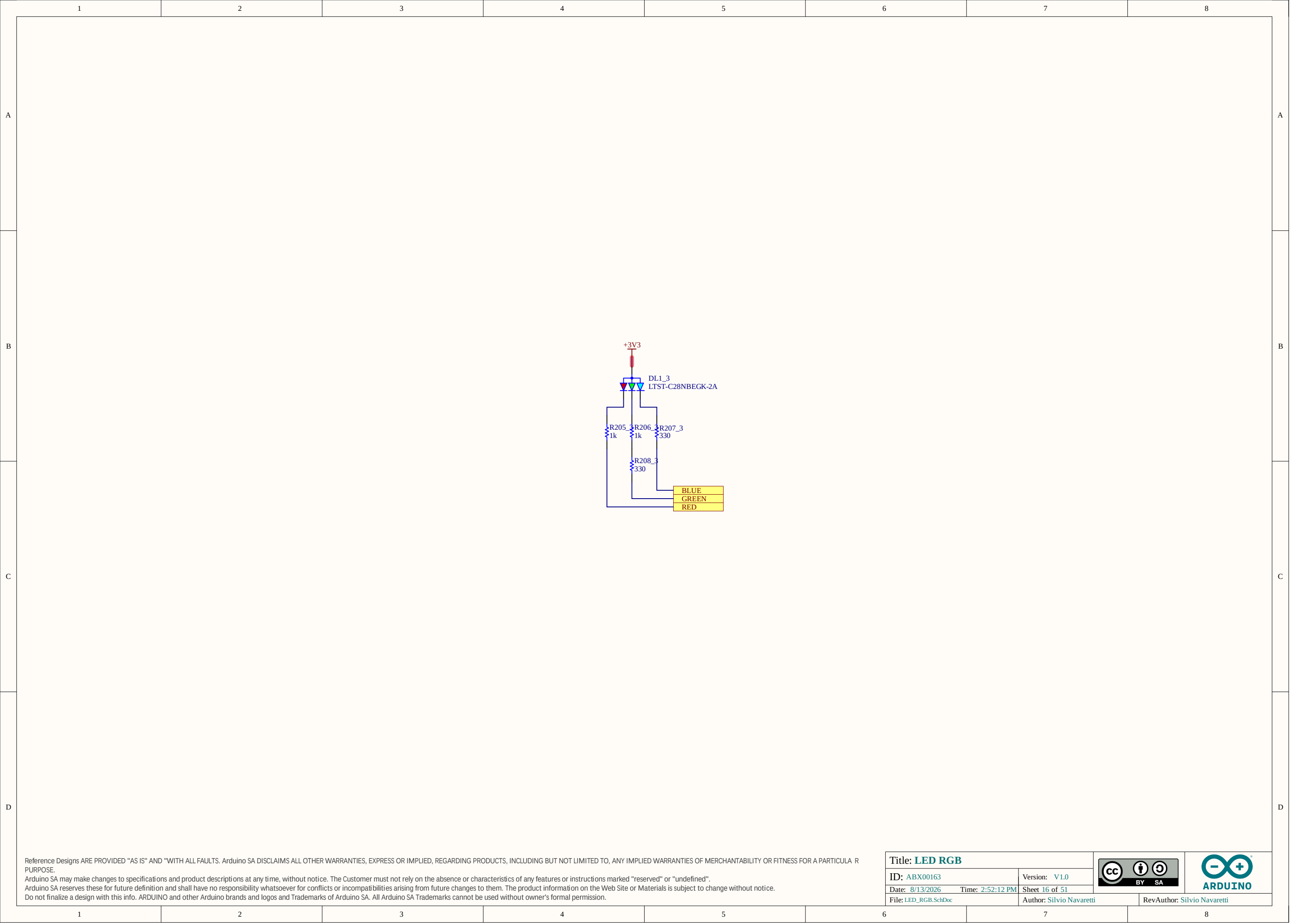
Date: 8/13/2026

Time: 2:52:11 PM

Sheet 16 of 51

File: LED_RGB.SchDoc

Author: [Silvio Navaretti](#)RevAuthor: **Silvio Navaretti**



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A

A

B

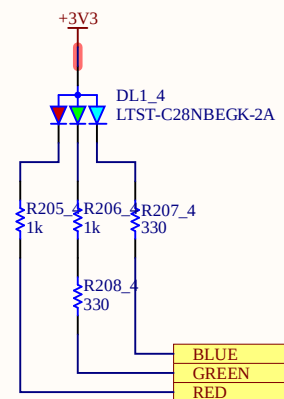
B

C

C

D

D



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Title: LED RGB

ID: ABX00163

Version: V1.0

Date: 8/13/2026

Time: 2:52:13 PM

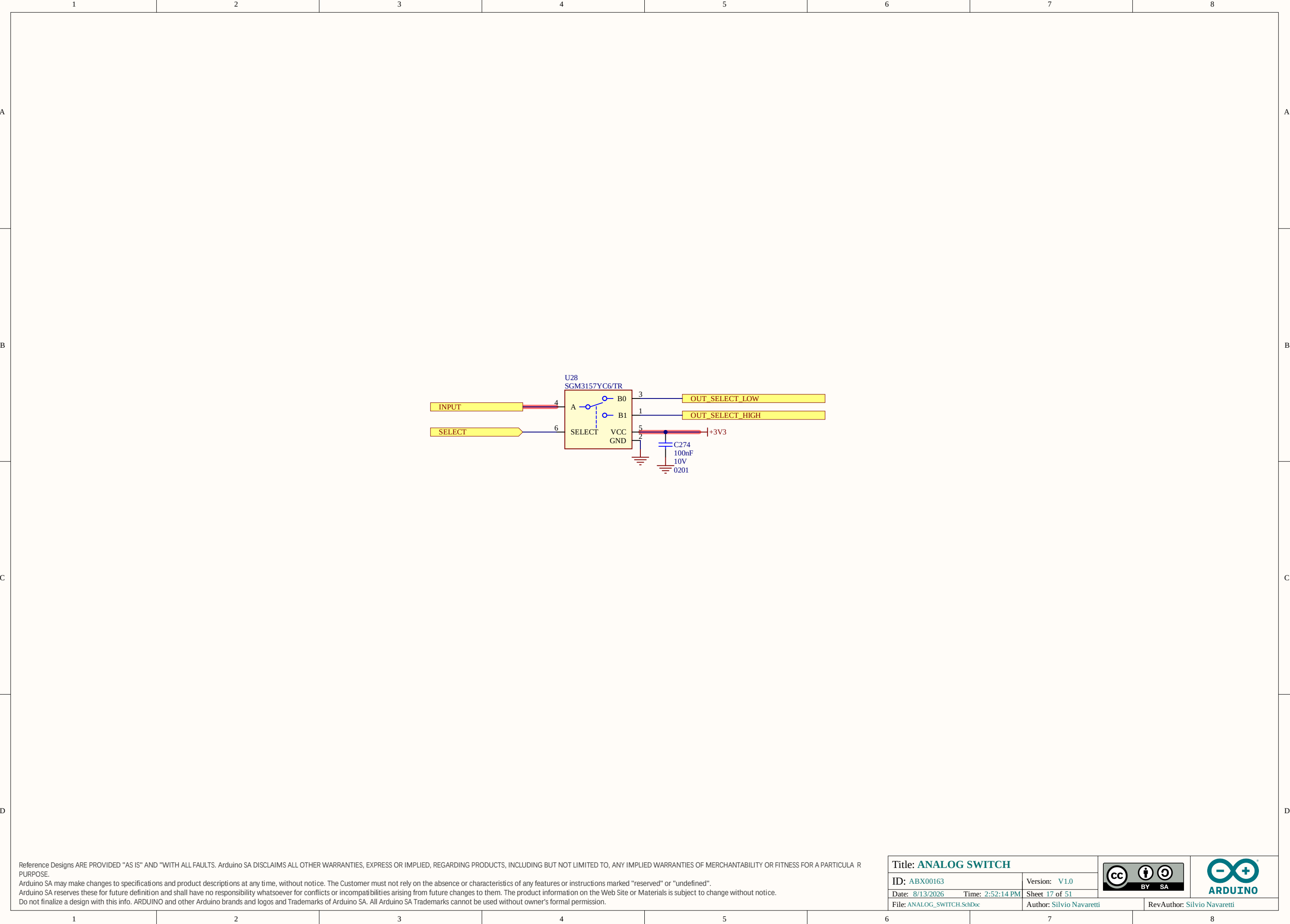
Sheet 16 of 51

File: LED_RGB.SchDoc

Author: **Silvio Navaretti**

RevAuthor: Silvio Navaretti





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1

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5

6

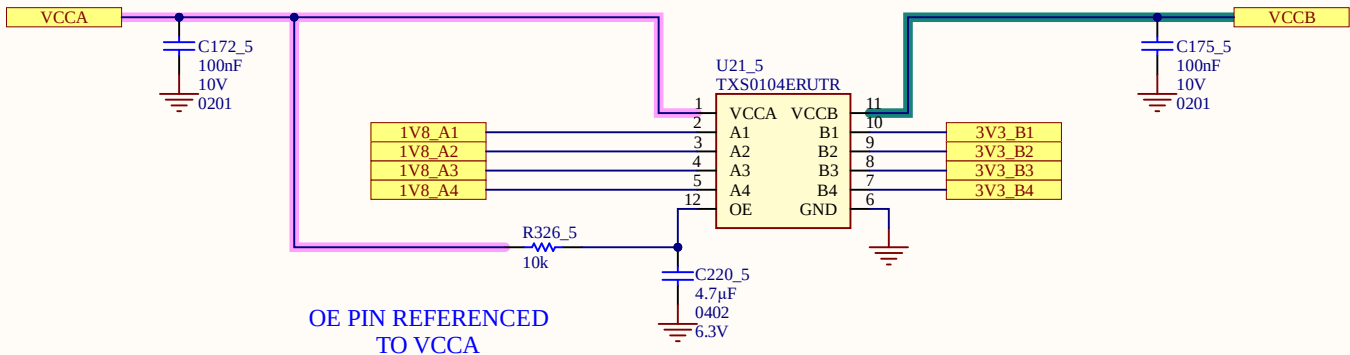
7

8

LEVEL TRANSLATOR
BIDIRECTIONAL 110Mbps (push pull), 1.2Mbps (open drain)
 $V_{CCA} \leq V_{CCB}$

A SIDE
1.4V to 3.6V
ESD 2kV Human body model

B SIDE
1.65V to 5.5V
ESD ±6kV Air Discharge

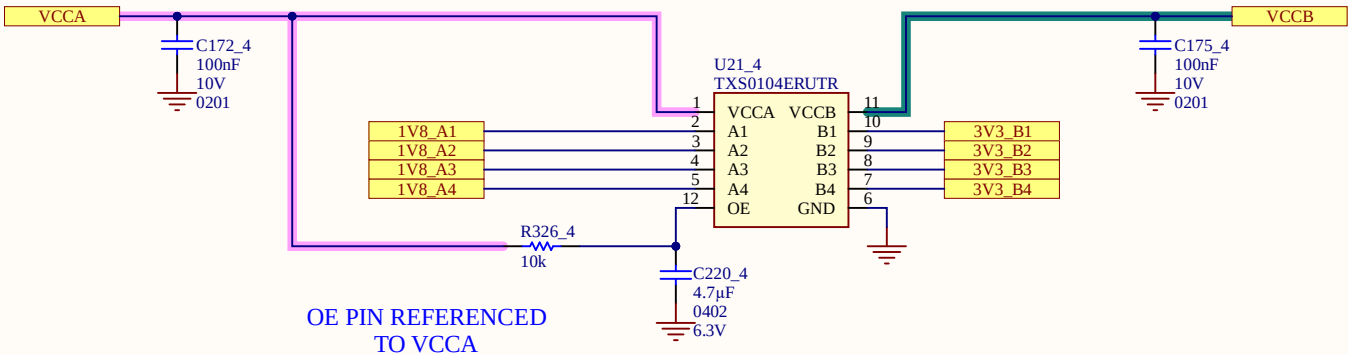


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LEVEL TRANSLATOR
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 $V_{CCA} \leq V_{CCB}$

A SIDE
1.4V to 3.6V
ESD 2kV Human body model

B SIDE
1.65V to 5.5V
ESD ±6kV Air Discharge

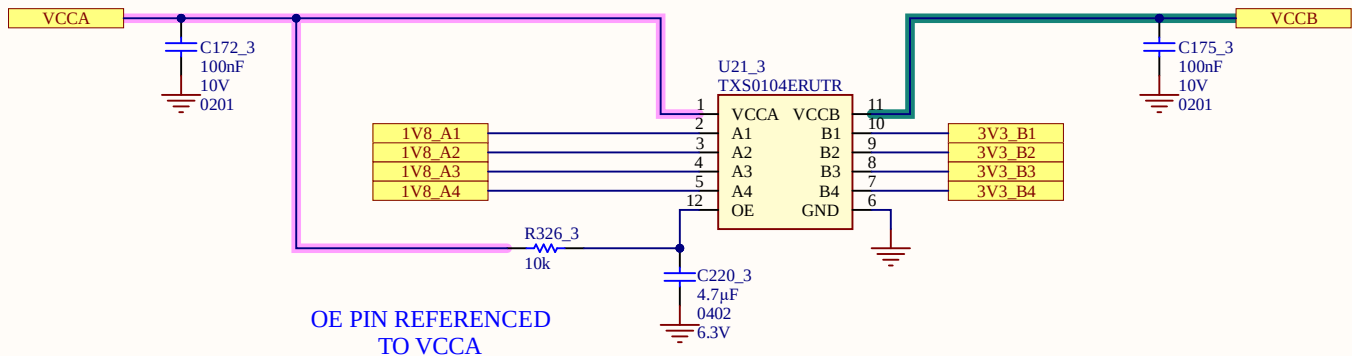


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LEVEL TRANSLATOR
BIDIRECTIONAL 110Mbps (push pull), 1.2Mbps (open drain)
 $V_{CCA} \leq V_{CCB}$

A SIDE
1.4V to 3.6V
ESD 2kV Human body model

B SIDE
1.65V to 5.5V
ESD ±6kV Air Discharge

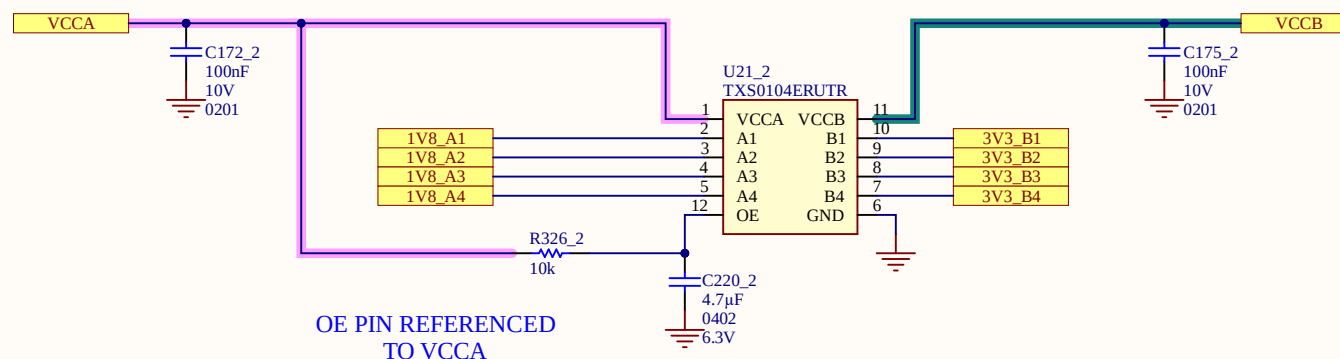


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LEVEL TRANSLATOR
 BIDIRECTIONAL 110Mbps (push pull), 1.2Mbps (open drain)
 $V_{CCA} \leq V_{CCB}$

A SIDE
1.4V to 3.6V
ESD 2kV Human body model

B SIDE
1.65V to 5.5V
ESD $\pm 6\text{kV}$ Air Discharge



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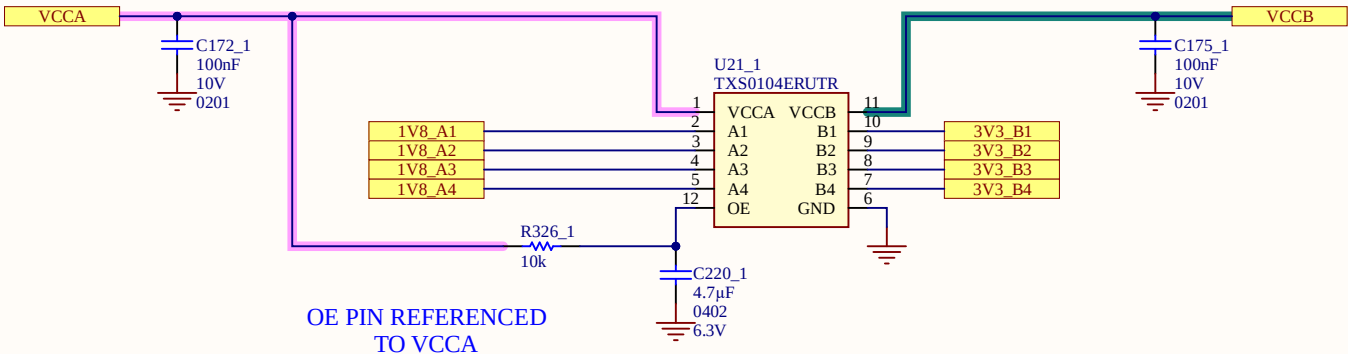
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Title: TRANSLATOR 4CH			
ID: ABX00163	Version: V1.0		
Date: 8/13/2026 Time: 2:52:18 PM	Sheet 18 of 51		
File: TRANSLATOR 4CH.SchDoc		Author: Silvio Navaretti	RevAuthor: Silvio Navaretti

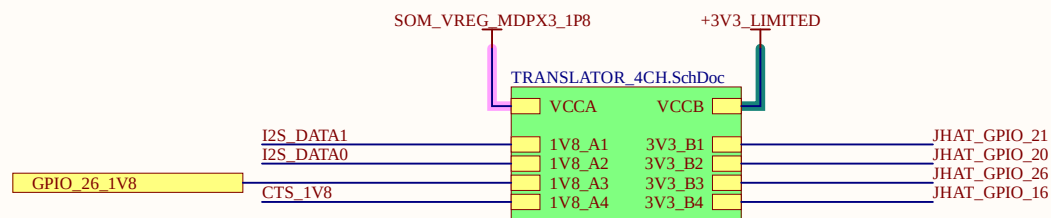
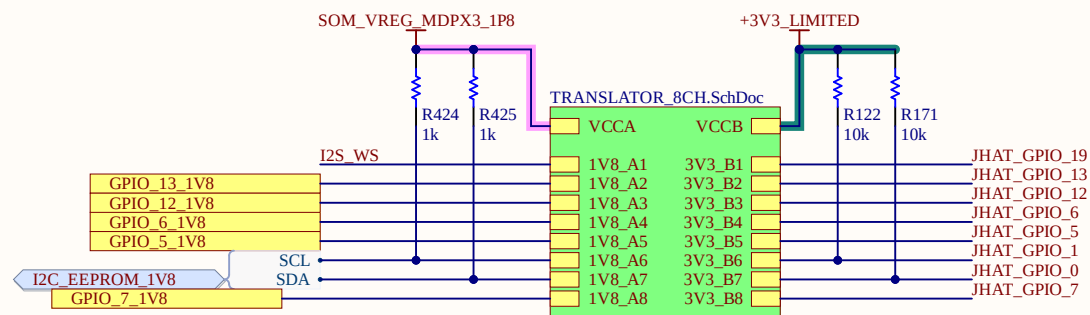
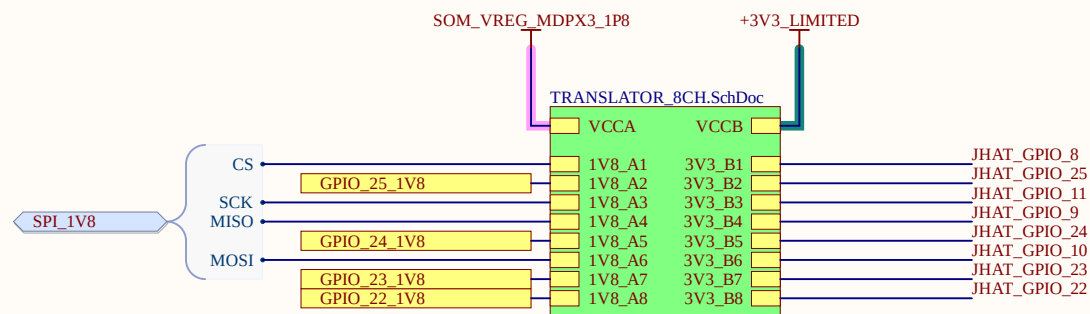
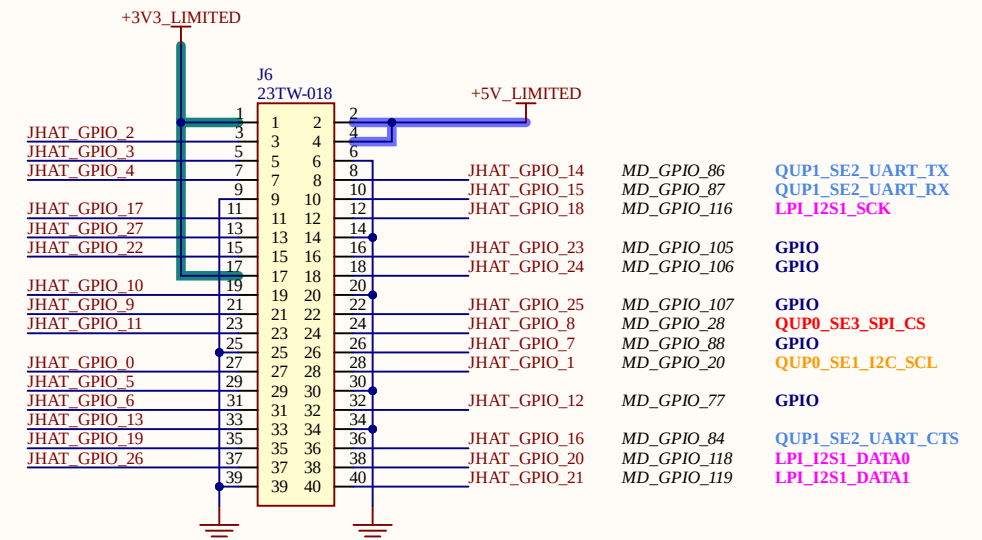
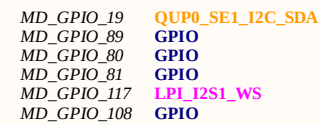
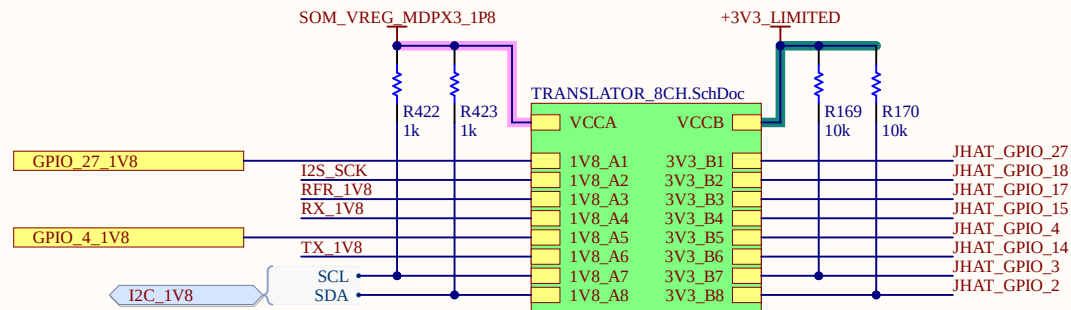
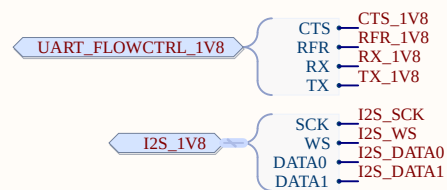
LEVEL TRANSLATOR
BIDIRECTIONAL 110Mbps (push pull), 1.2Mbps (open drain)
 $V_{CCA} \leq V_{CCB}$

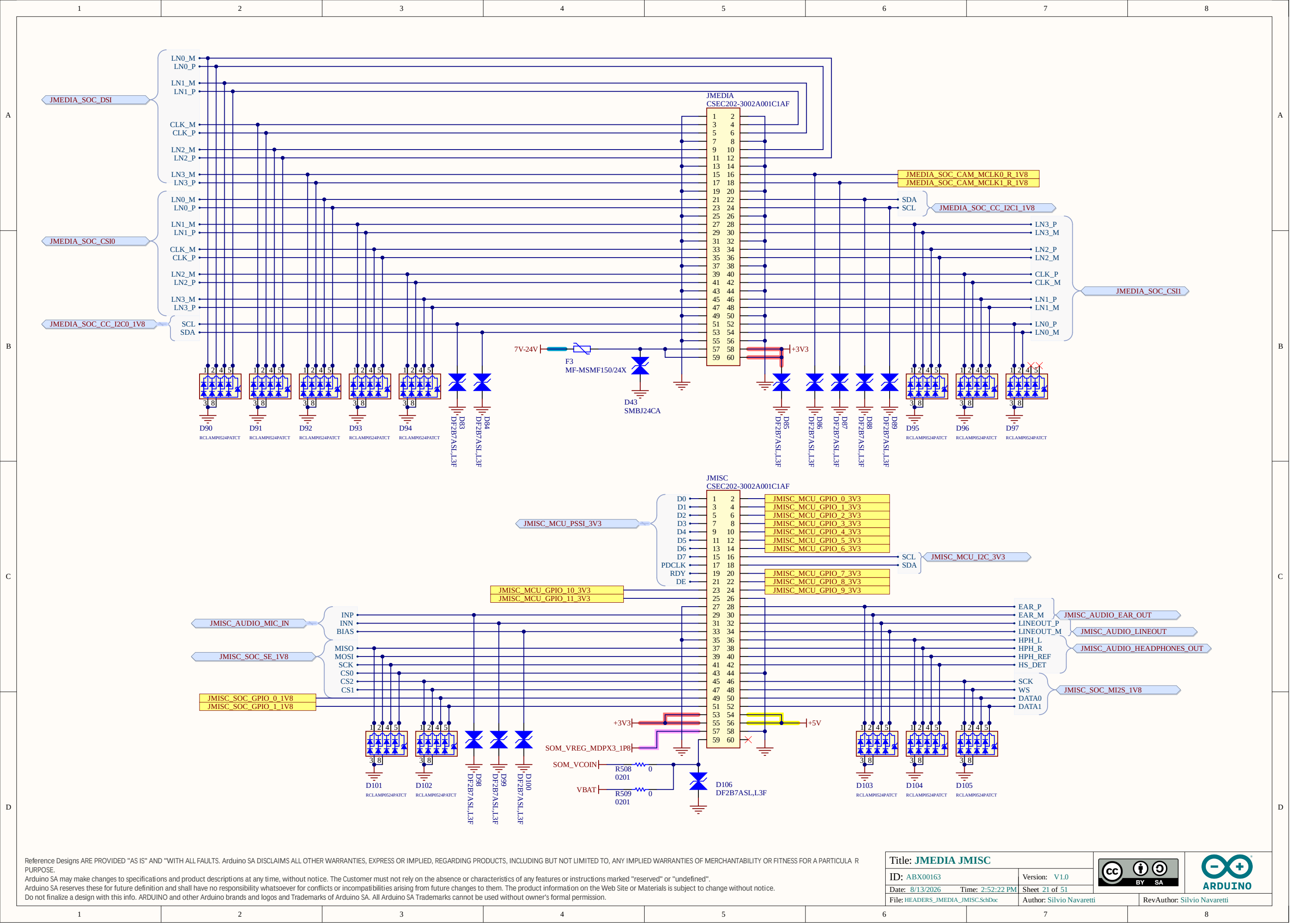
A SIDE
1.4V to 3.6V
ESD 2kV Human body model

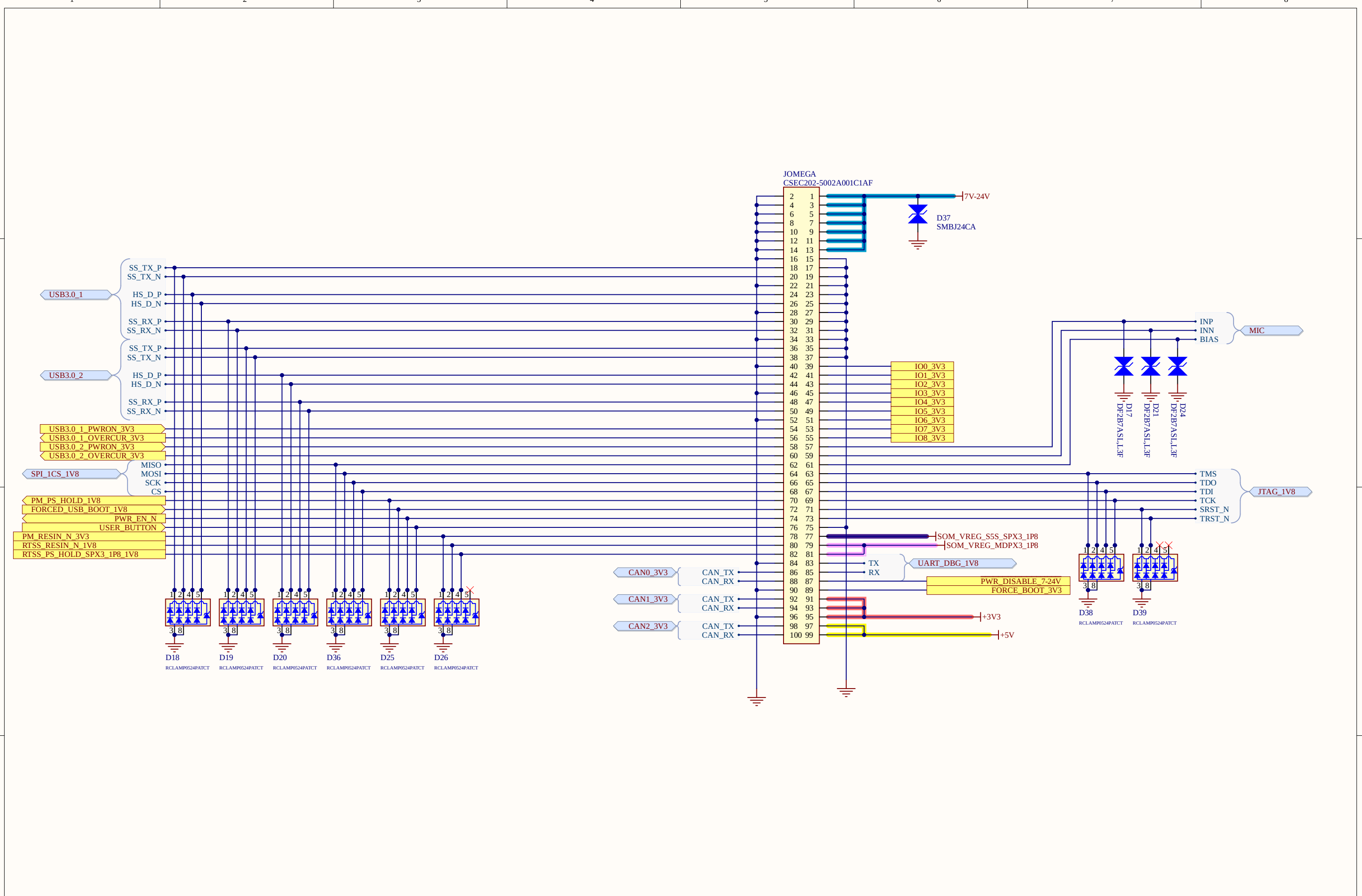
B SIDE
1.65V to 5.5V
ESD ±6kV Air Discharge

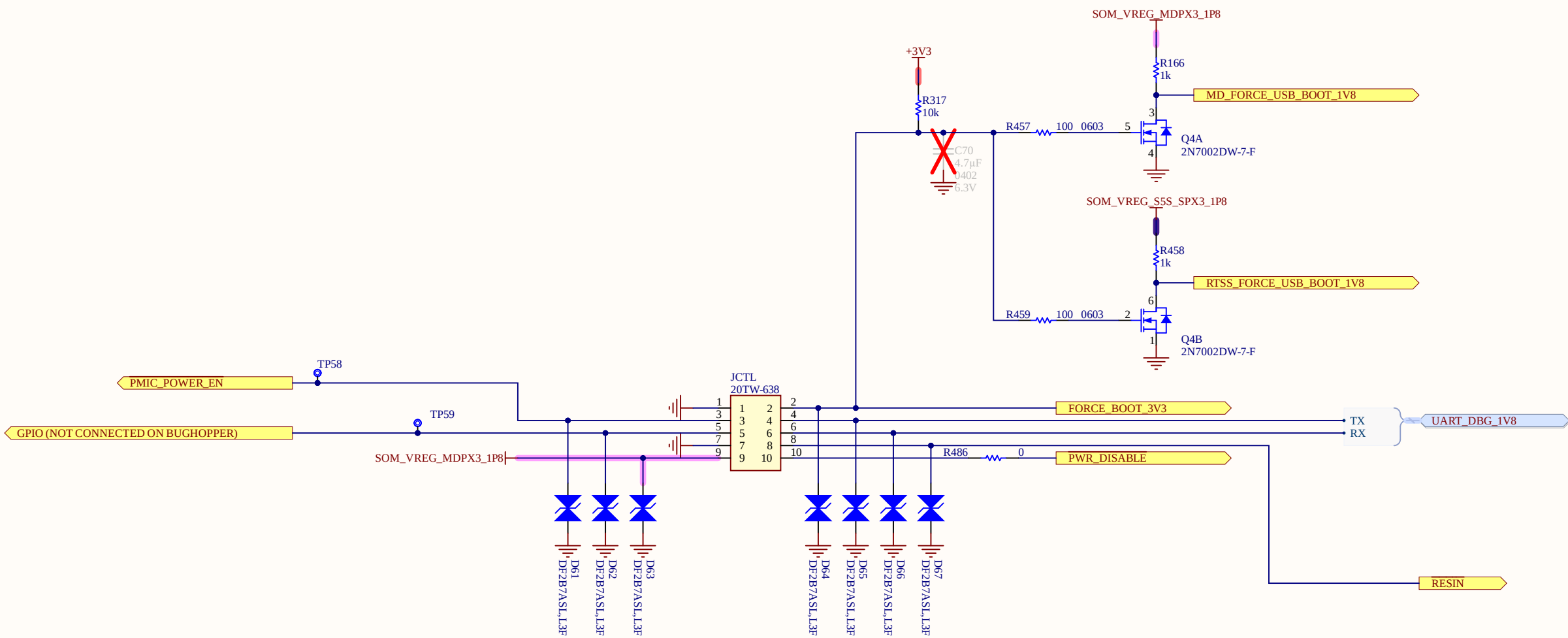


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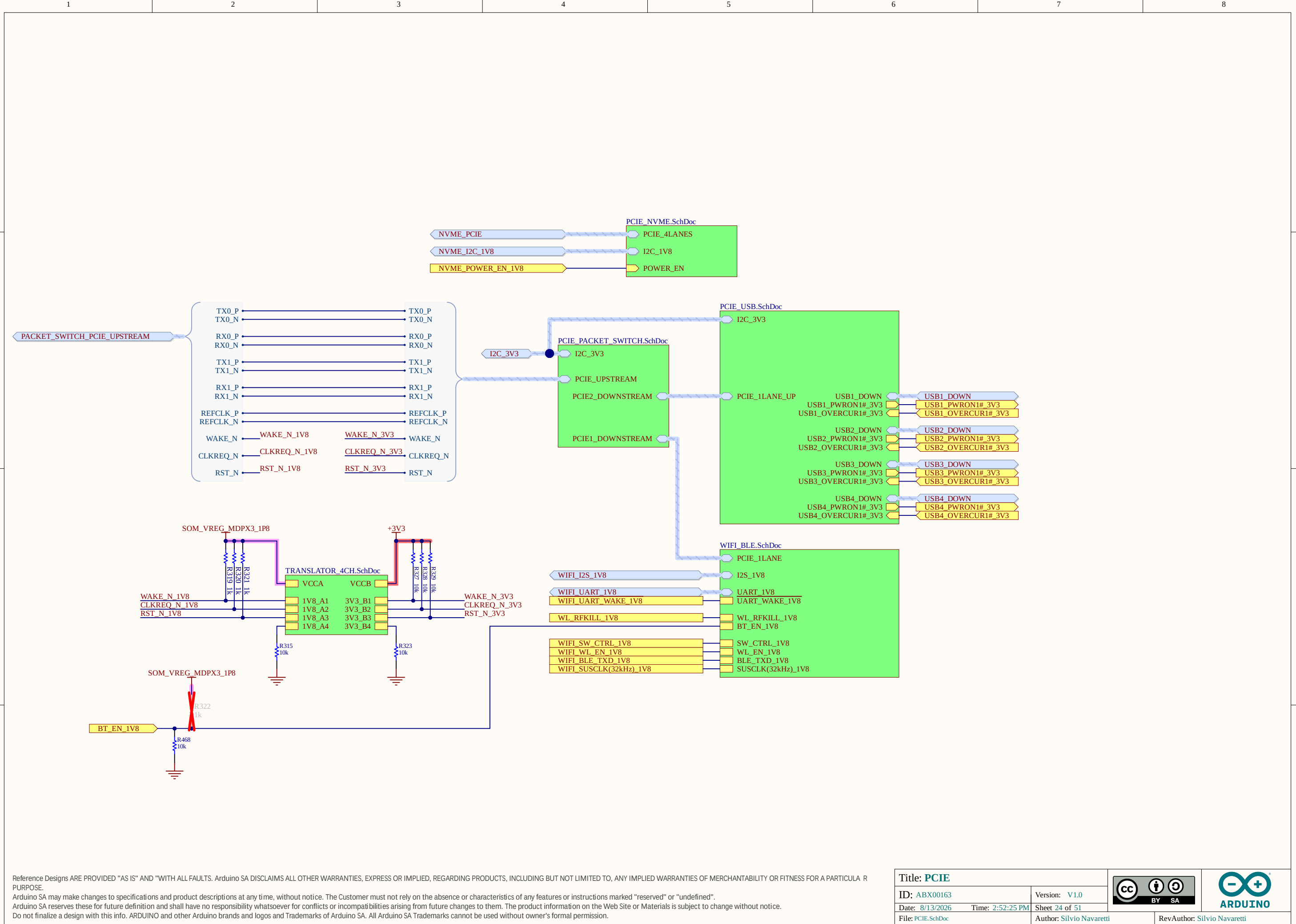






JCTL pin descriptions:

- Pin 2: FORCED_USB_BOOT_N -> when pulled LOW via an external open drain pin, the board should enter EDL mode on reboot
- Pin 8: RESIN_N -> when pulled LOW via an external open drain pin, the main processor should reboot (keeping voltage rails ON) -> hot reboot
- Pin 10: POWER_SWITCH_DISABLE_N -> when pulled LOW via an external open drain pin, the main power source should be gated -> cold reboot

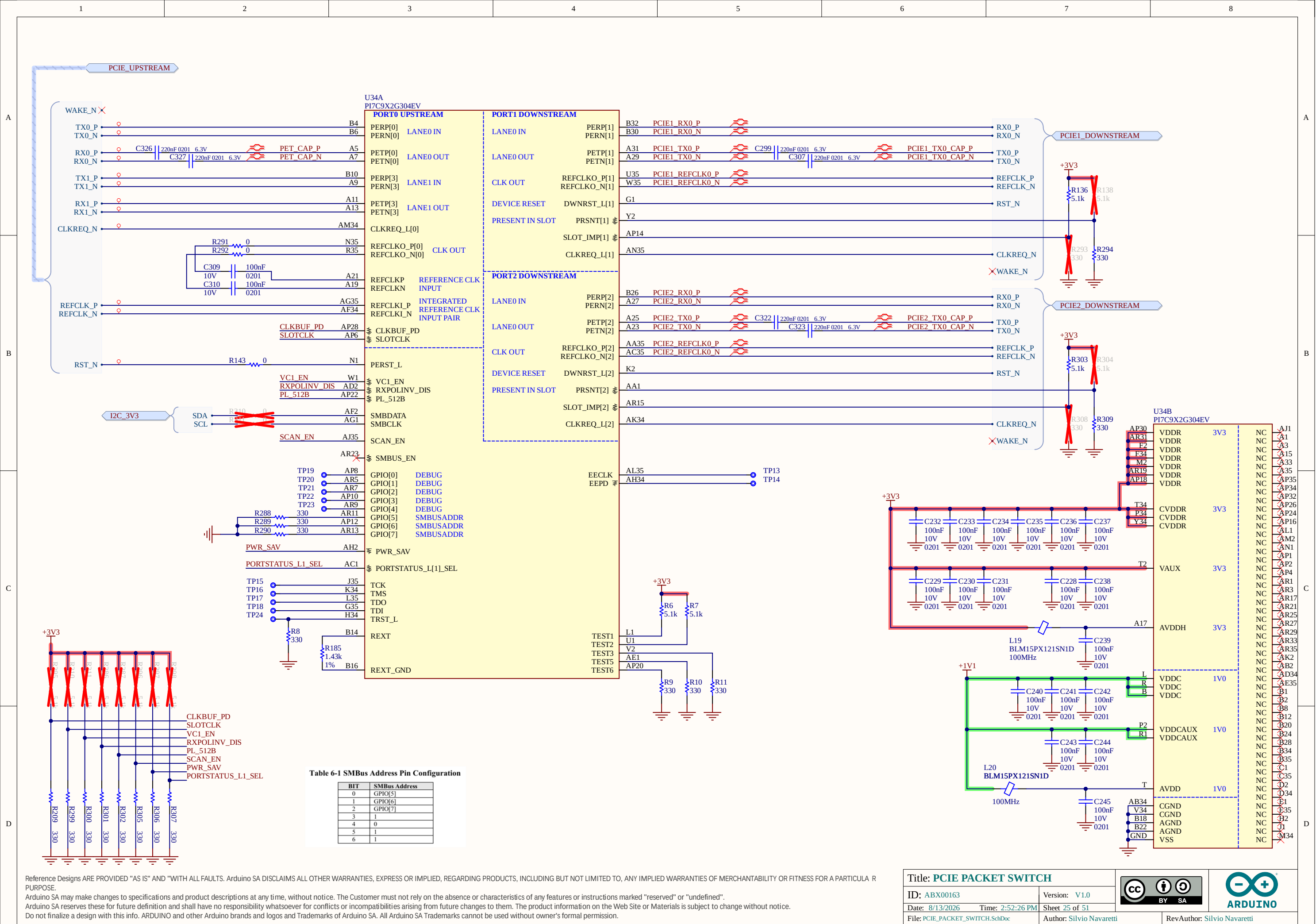


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Title: **PCIe PACKET SWITCH**

ID: ABX00163

Version: V1.0

Date: 8/13/2026

Time: 2:52:26 PM

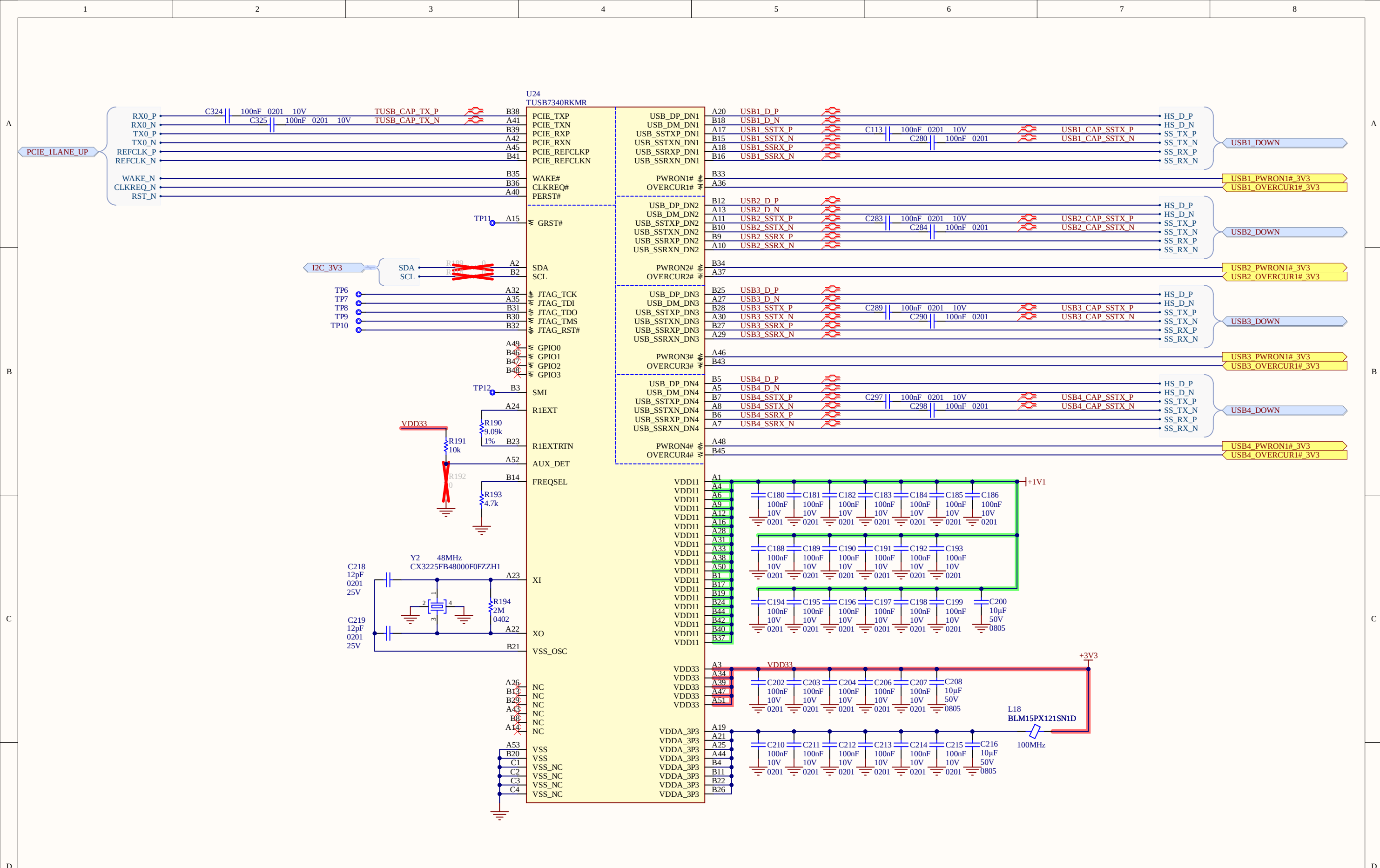
Sheet 25 of 51

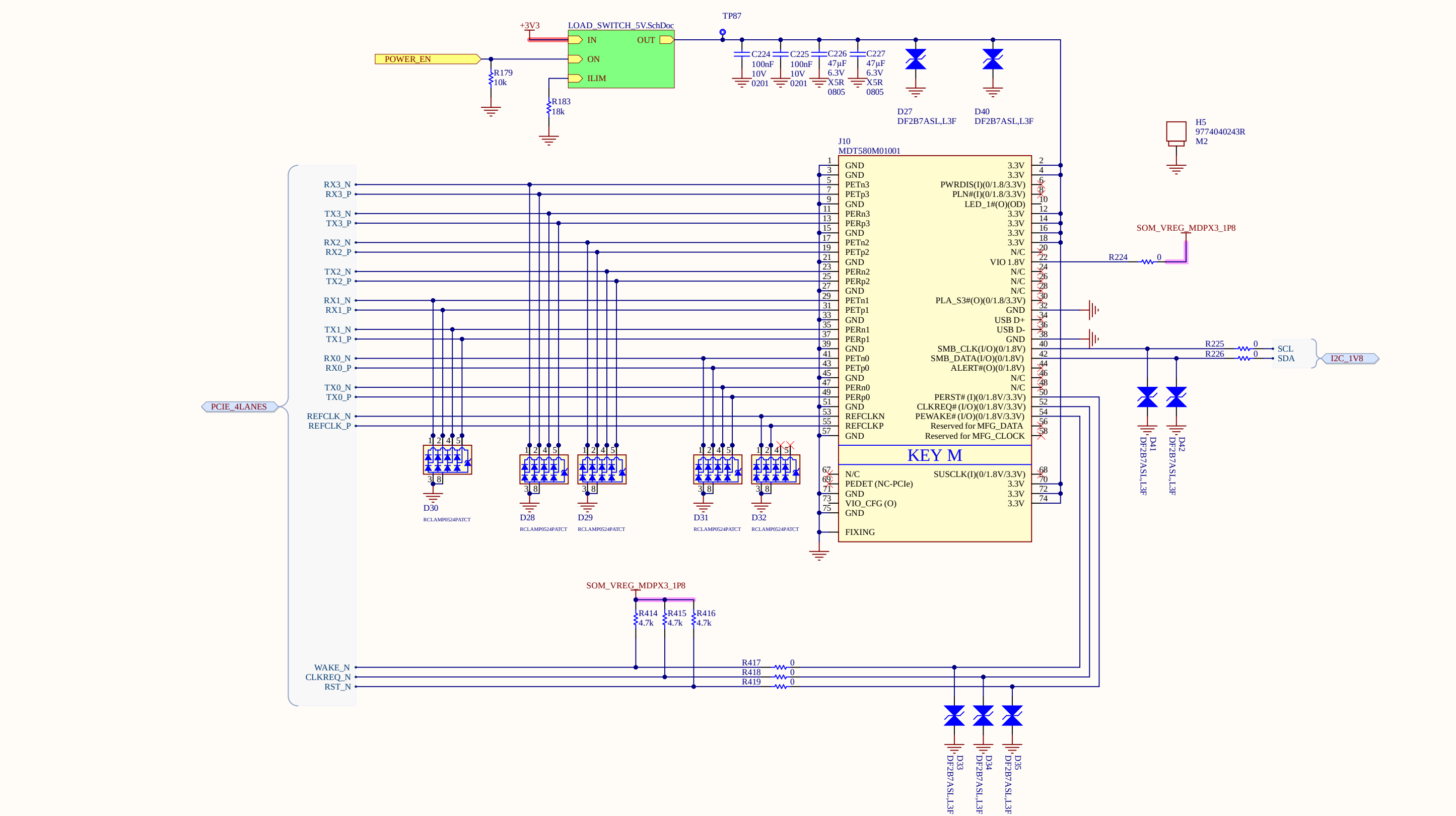
File: PCIe_PACKET_SWITCH.SchDoc

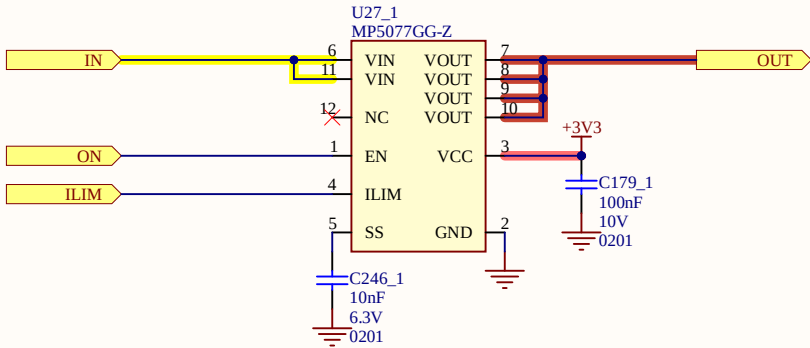
Author: Silvio Navaretti

RevAuthor: Silvio Navaretti









The pre-set current limit value can be calculated by below equation:

$$I_{Limit} = (1+R_{Limit}) \times S \quad (1)$$

S is the current sense ratio of MP5077, and this value is typically 82000 in $V_{IN}=3.6V$. The S is almost a constant value when Vin is changing from 1.2V to 5.5V, and when Vin is smaller than 1.2V, a step change will come to S value, the value will change from 82000 to about 80000. Meanwhile, when Vcc is changing, there is also a little shift on S value, for more information, please refer the curves in typical performance characteristics.

Soft-Start

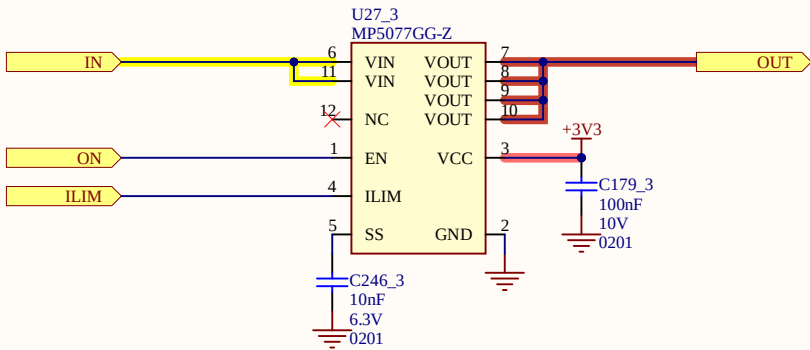
A capacitor connected to the SS pin determines the soft-start time. There is an internal 9μA constant current source charge SS cap and ramps up the voltage on the SS pin. The output voltage rises at 3 times the slew rate to SS voltage.

The soft-start time can be calculated by below equation:

$$T_{ss} (ms) = \frac{1}{3} \times \frac{V_{OUT} (V) \cdot C_{SS} (nF)}{I_{ss} (\mu A)} \quad (2)$$

T_{ss} is the soft-start time, I_{ss} is internal 9μA constant current, C_{SS} is external soft-start cap.

The suggestion minimum SS cap should be bigger than 4.7nF. If the SS pin is floated or SS cap is too small, the Vout rising time will be just limited by power MOS charge time.



The pre-set current limit value can be calculated by below equation:

$$I_{Limit} = (1+R_{Limit}) \times S \quad (1)$$

S is the current sense ratio of MP5077, and this value is typically 82000 in $V_{IN}=3.6V$. The S is almost a constant value when Vin is changing from 1.2V to 5.5V, and when Vin is smaller than 1.2V, a step change will come to S value, the value will change from 82000 to about 80000. Meanwhile, when Vcc is changing, there is also a little shift on S value, for more information, please refer the curves in typical performance characteristics.

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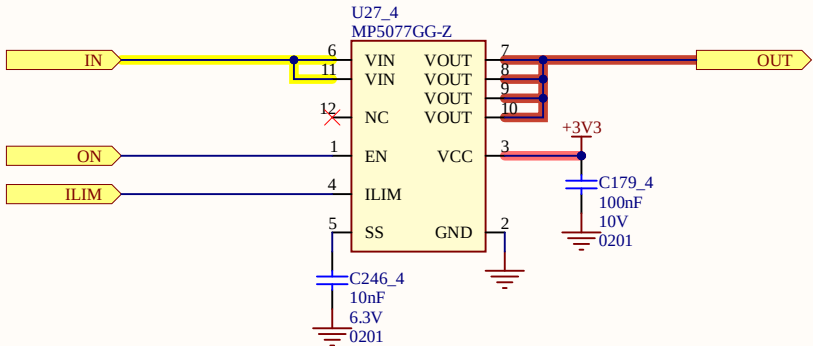
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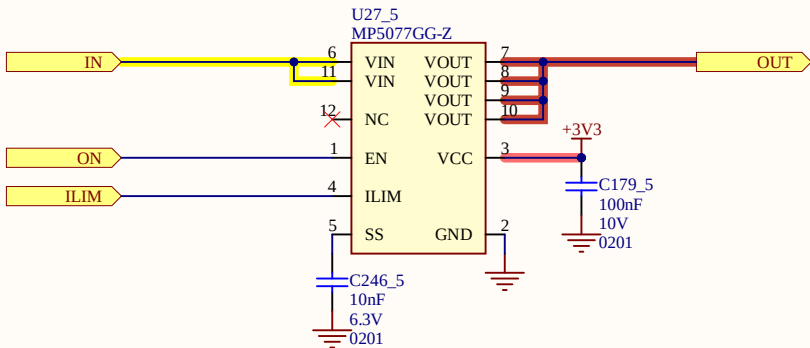
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Soft-Start

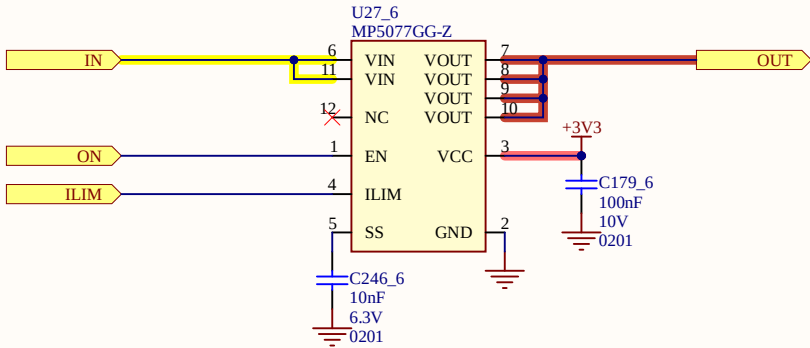
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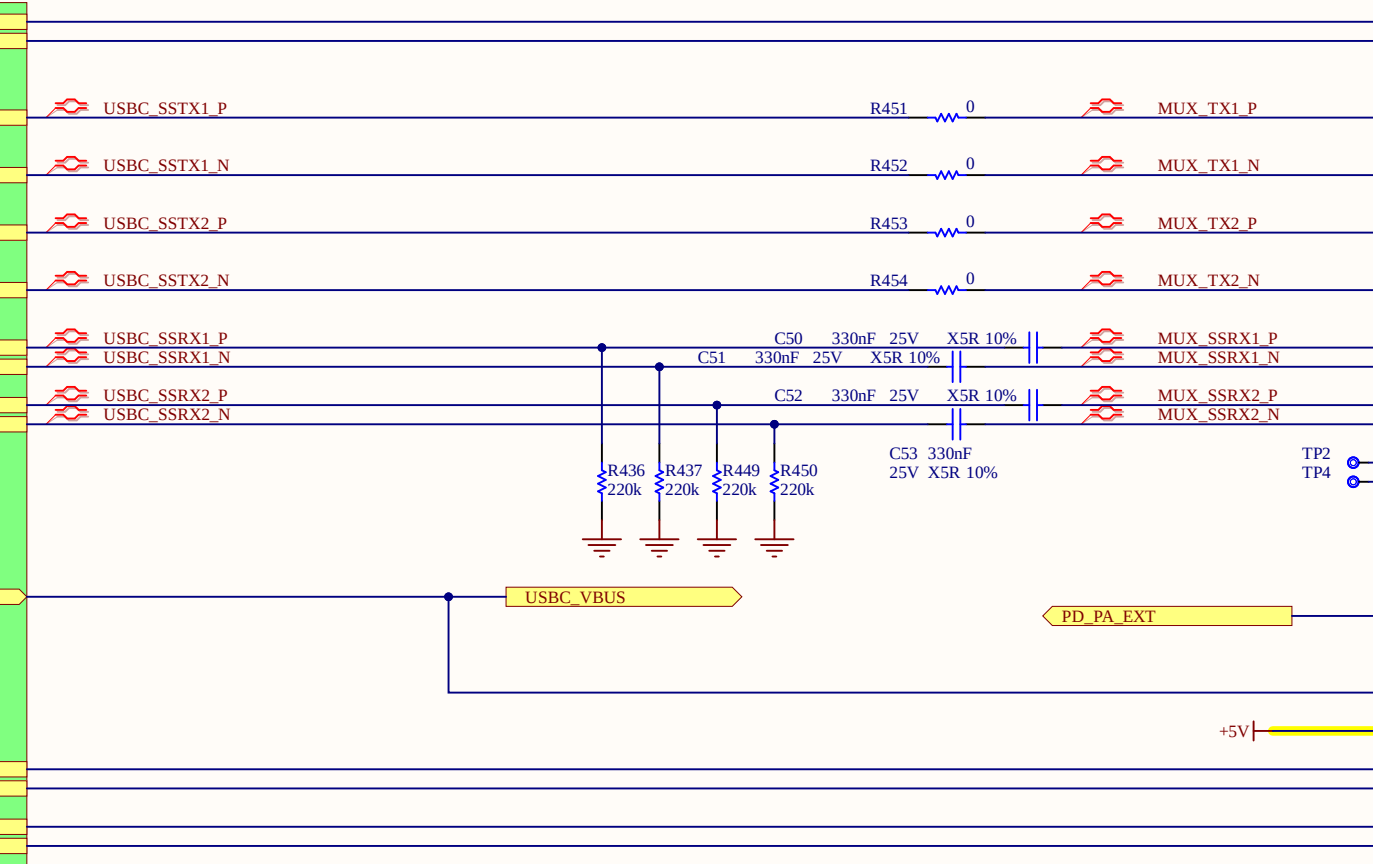
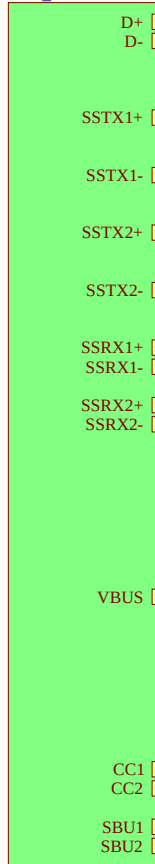
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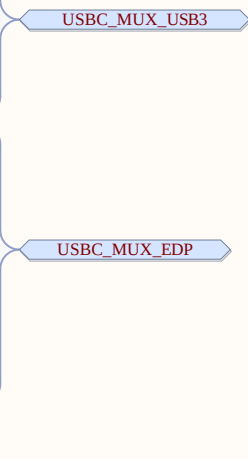
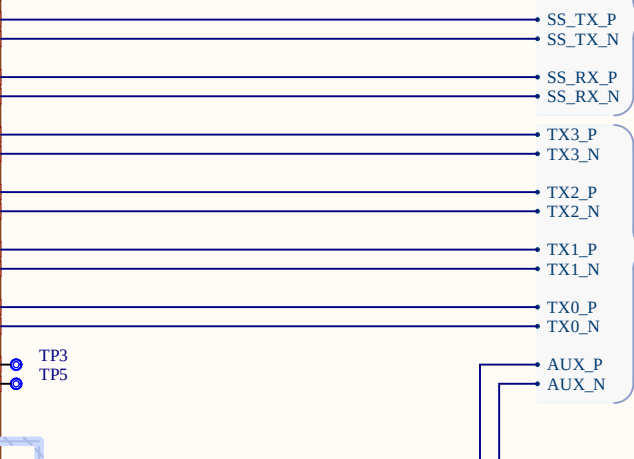
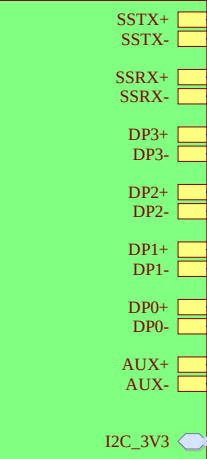
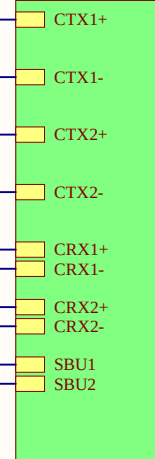
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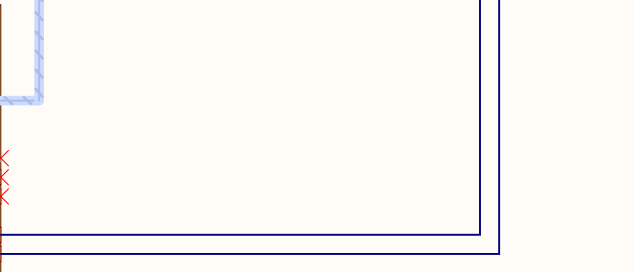
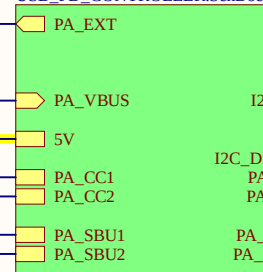
USB_USBC.SchDoc



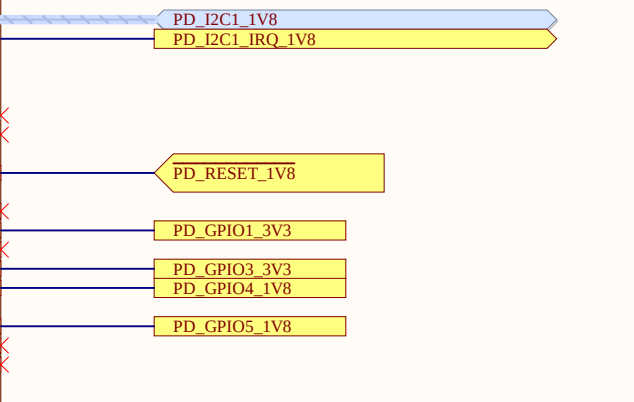
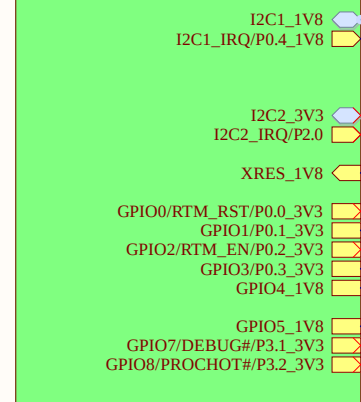
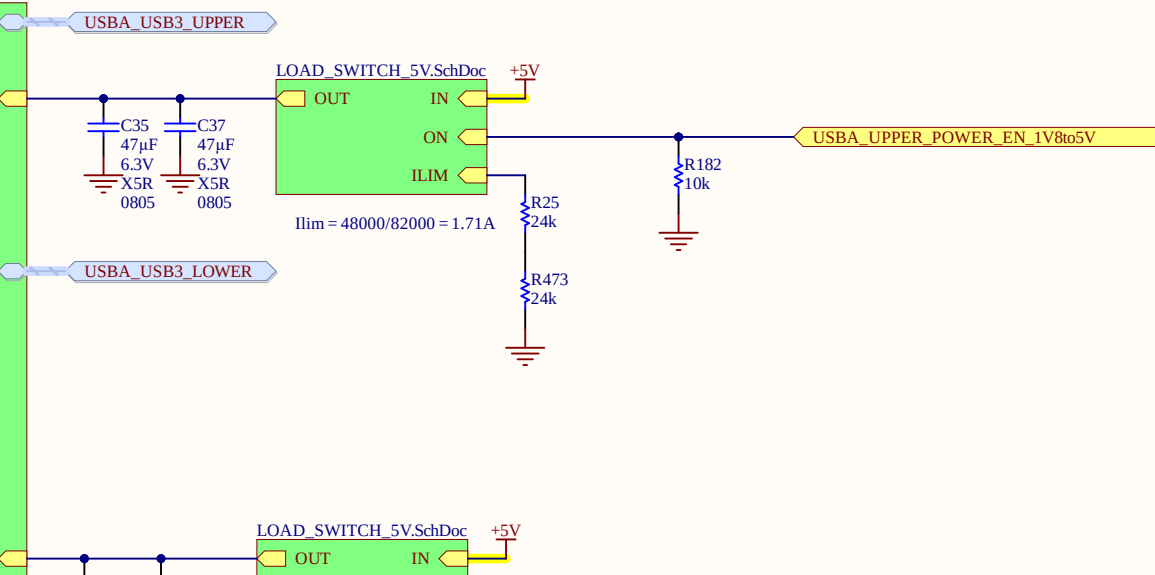
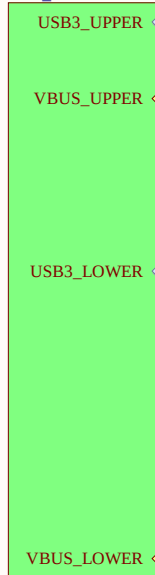
USB_MUX.SchDoc



USB_PD_CONTROLLER.SchDoc



USB_USBA.SchDoc



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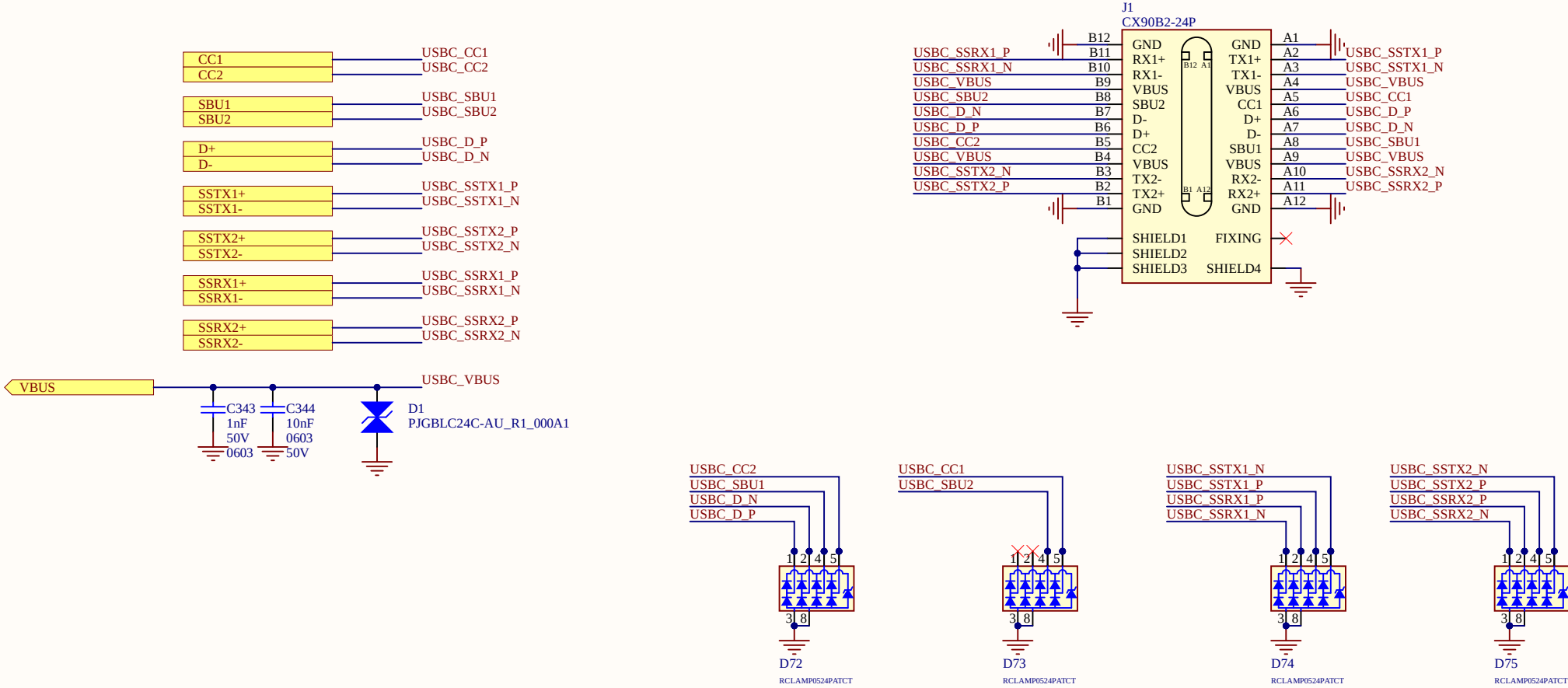
Version: V1.0

Sheet 30 of 51

Author: Silvio Navaretti

RevAuthor: Silvio Navaretti





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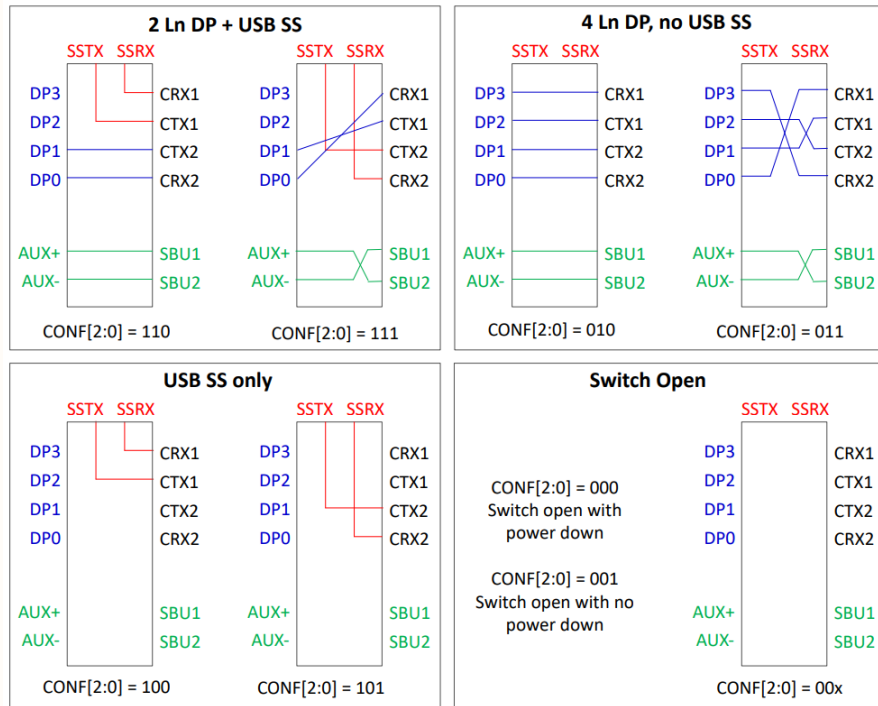


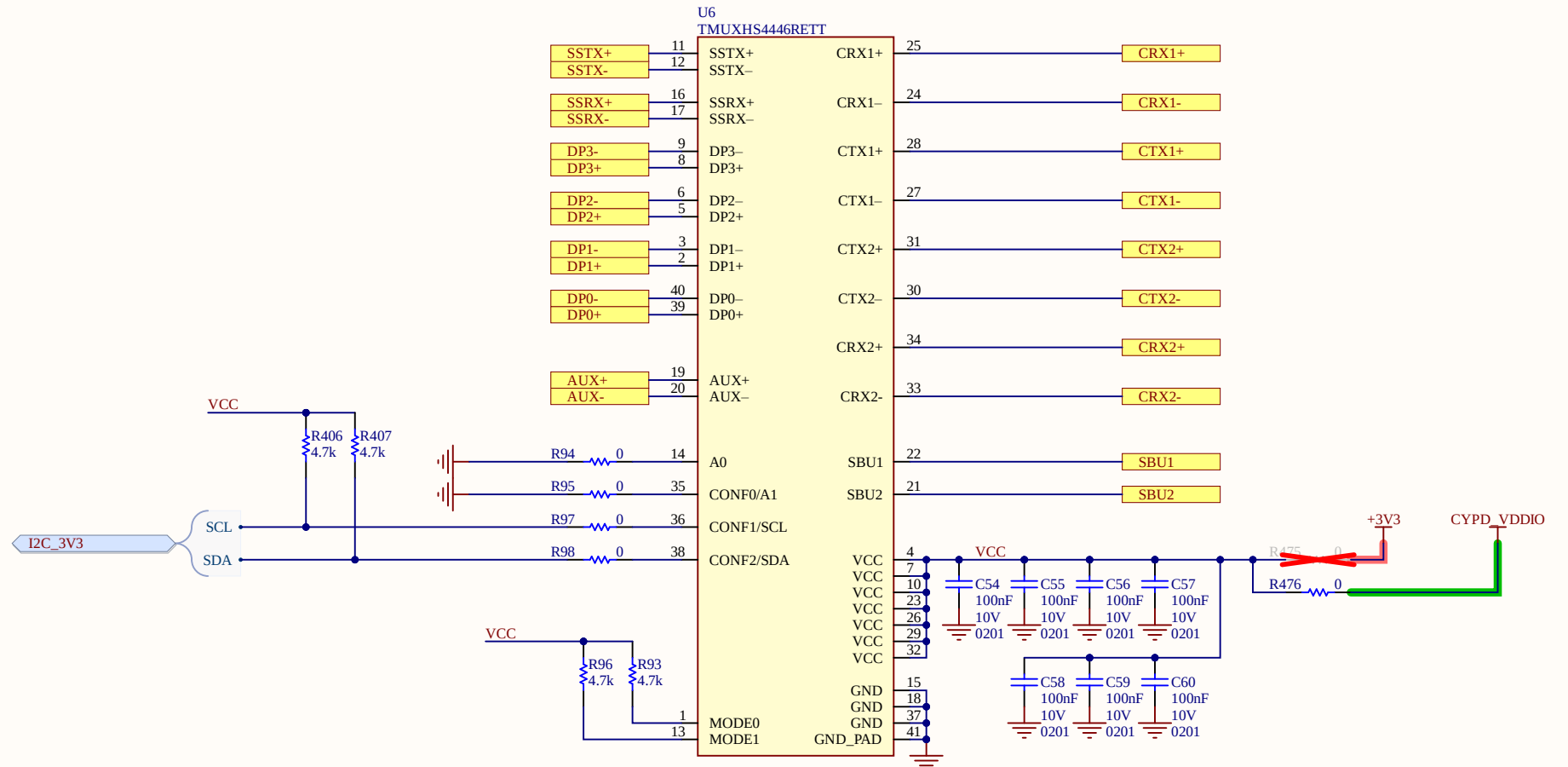
Figure 6-2. TMUXHS4446 Signal Flow Diagrams in Different Configurations for Source Applications

MODE0	1	CTRL	Control mode selection MODE0 = 1, I ² C control MODE0 = 0, GPIO or pin control through CONF[2:0]
MODE1	13	CTRL	I ² C logic level control (MODE0 = 1) MODE1 = 0, 1.8V I ² C logic level MODE1 = 1, 3.3V I ² C logic level
CONF0	35	CTRL	GPIO control (MODE0 = 0) Switch configuration control for high-speed and low-speed pins. Refer to the Device Functional Modes section for details.
A1		CTRL	I ² C control (MODE0 = 1) Configurable I ² C target address bit
CONF1	36	CTRL	GPIO control (MODE0 = 0) Switch configuration control for high-speed and low-speed pins. Refer to the Device Functional Modes section for details.
SCL		CTRL	I ² C control (MODE0 = 1) I ² C clock input
CONF2	38	CTRL	GPIO control (MODE0 = 0) Switch configuration control for high-speed and low-speed pins. Refer to the Device Functional Modes section for details.
SDA		CTRL	I ² C control (MODE0 = 1) I ² C data input
A0	14	CTRL	I ² C control (MODE0 = 1) Configurable I ² C target address bit

Table 6-2 shows I2C Register sets. A1 and A0 (Byte 1, bits 2 and 1) are set by pins 35 and 14. CONF[2-0] (Byte 3, bits 2-0) sets the device configurations in I2C mode.

Table 6-2. I²C Control

Byte # & Description	Register Bits							
	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Byte 1, I ² C Secondary Target address	1	0	1	0	1	A1	A0	0/1 (W/R)
Byte 2, Device ID (read only)	0	0	0	0	0	0	0	0
Byte 3, Selection control (read/write)	0	0	0	0	0	CONF[2]	CONF[1]	CONF[0]

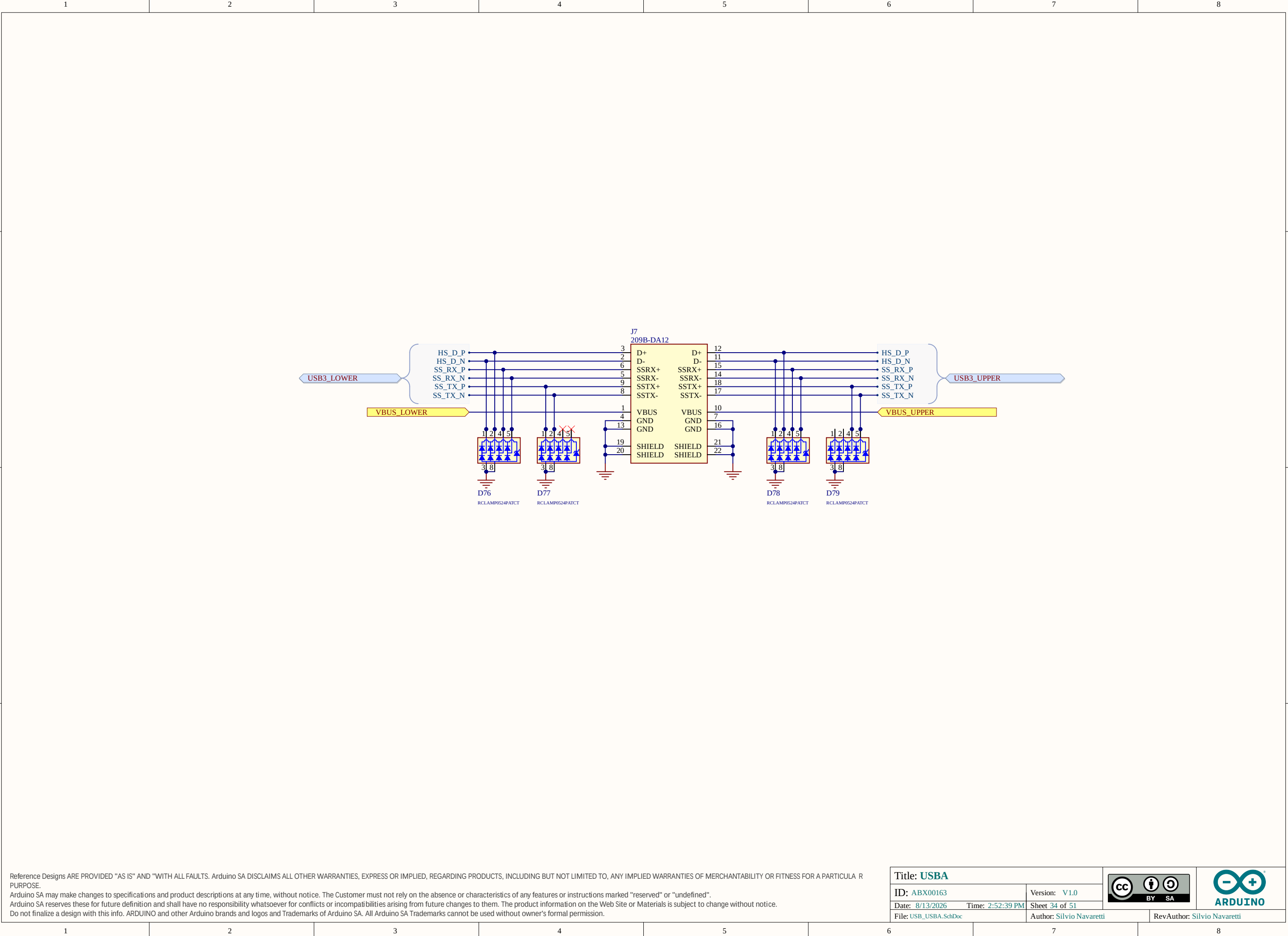


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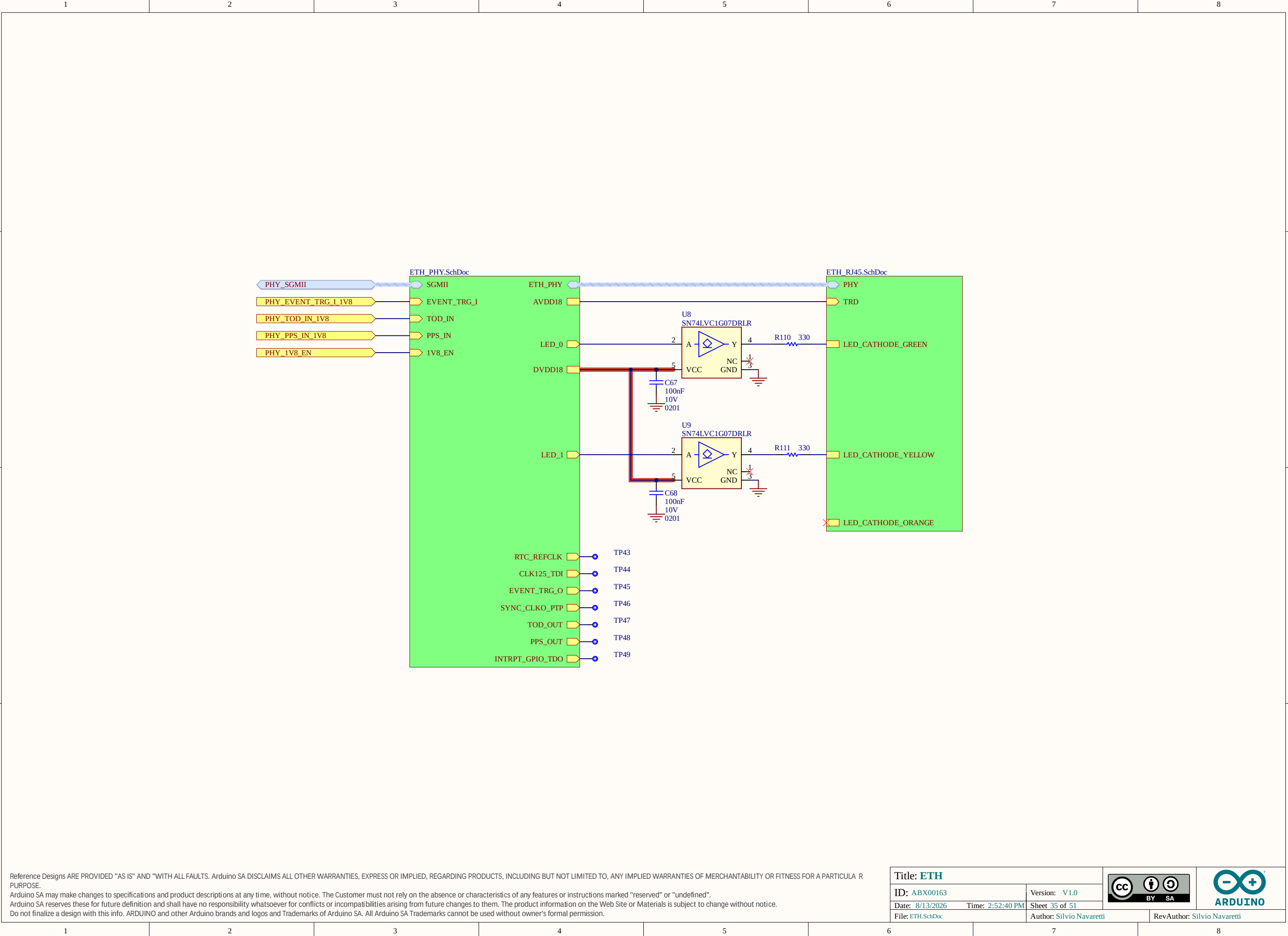


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Time: 2:52:40 PM

Sheet 35 of 51

Author: Silvio Navaretti

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RevAuthor: Silvio Navaretti

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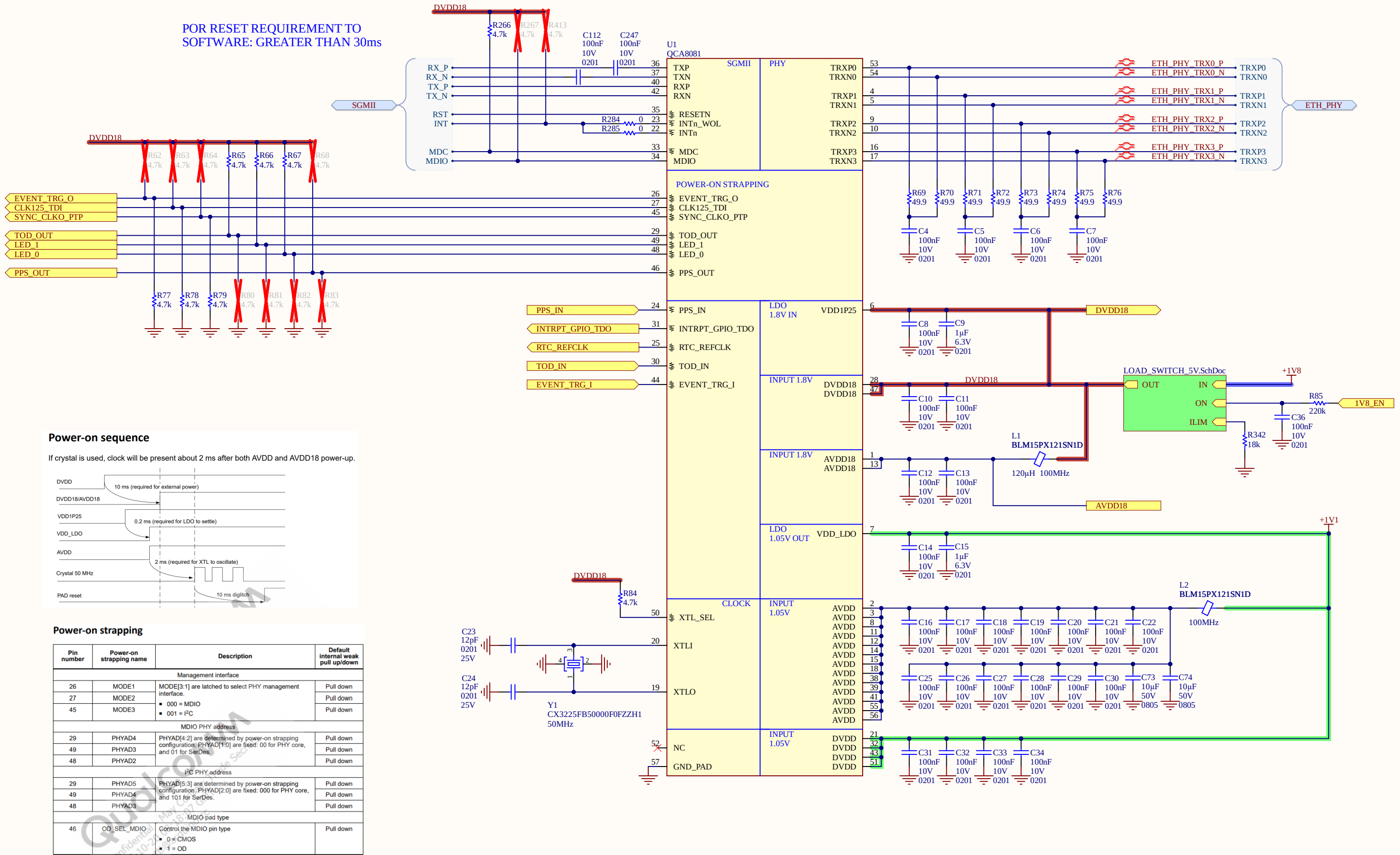
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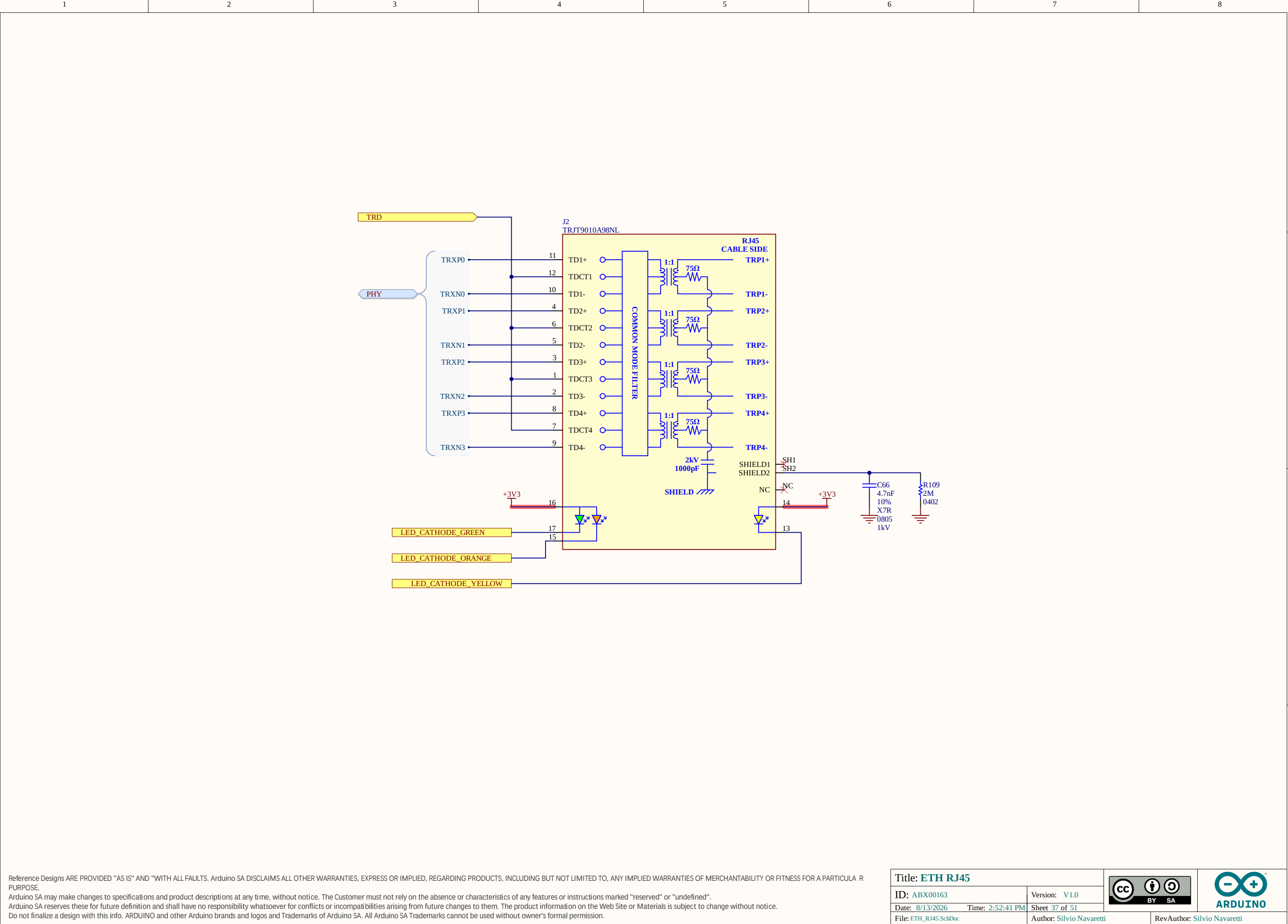
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POR RESET REQUIREMENT TO SOFTWARE: GREATER THAN 30ms





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Version: V1.0

Time: 2:52:41 PM

Author: Silvio Navaretti

Sheet 37 of 51

RevAuthor: Silvio Navaretti

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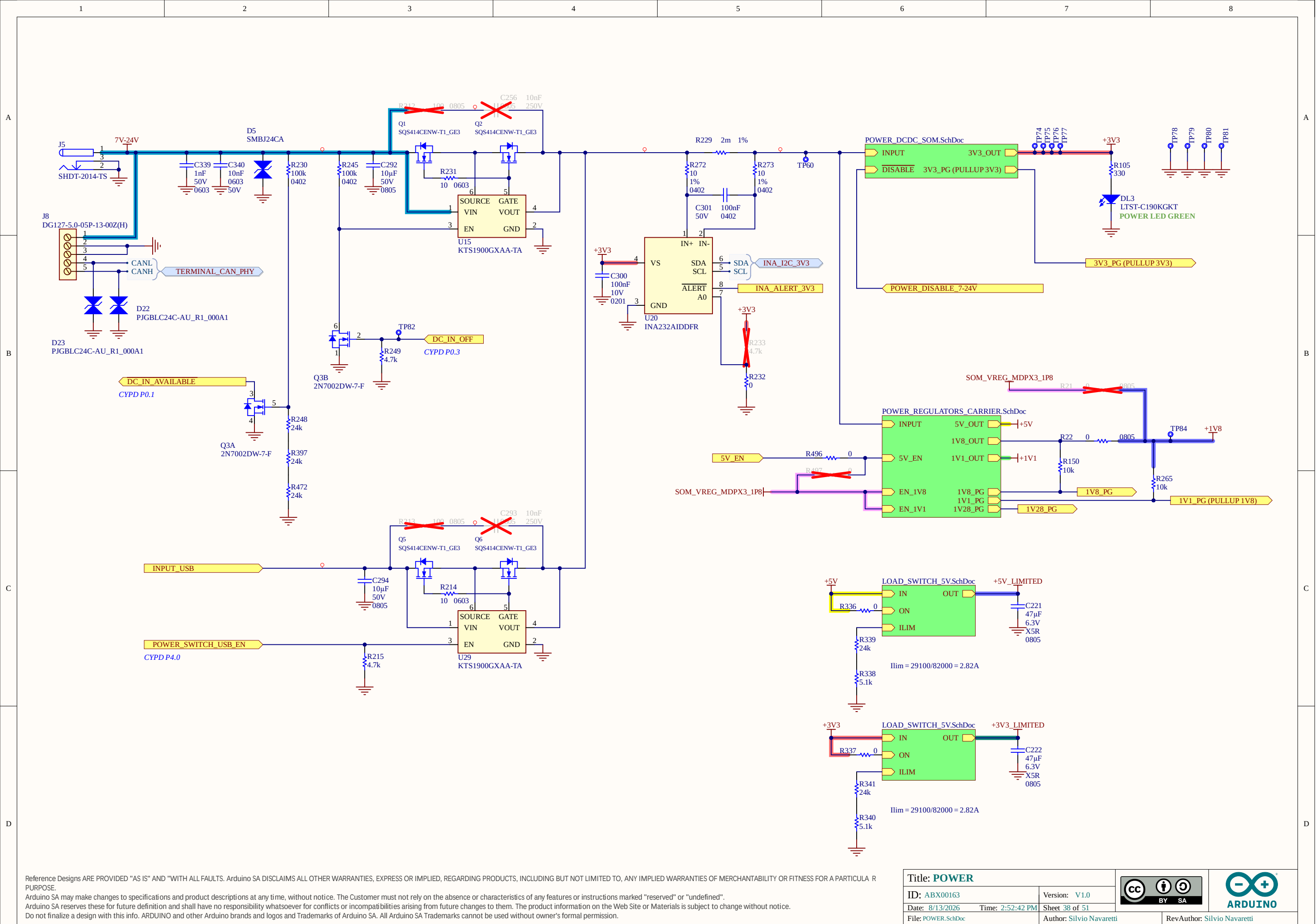
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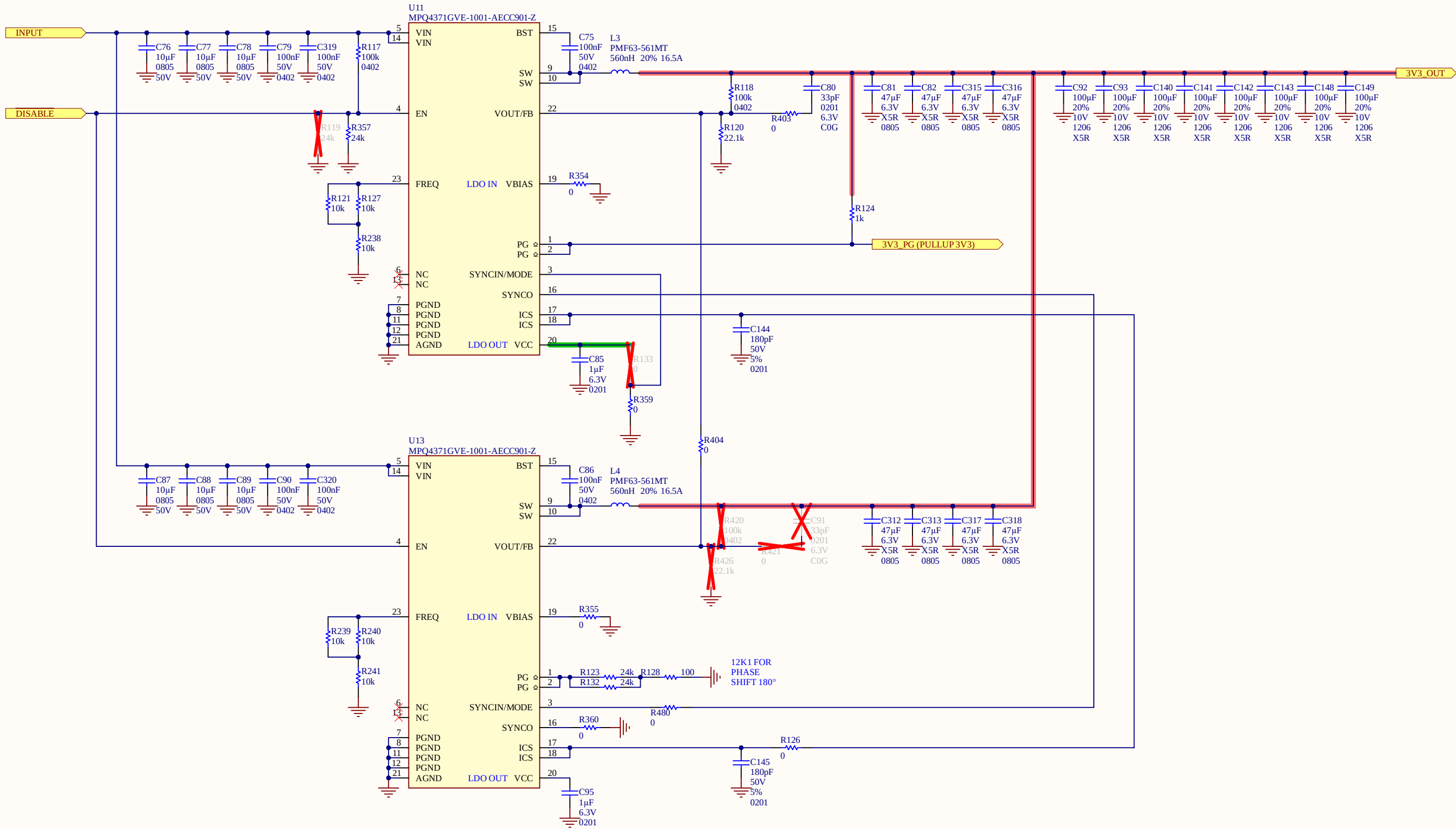


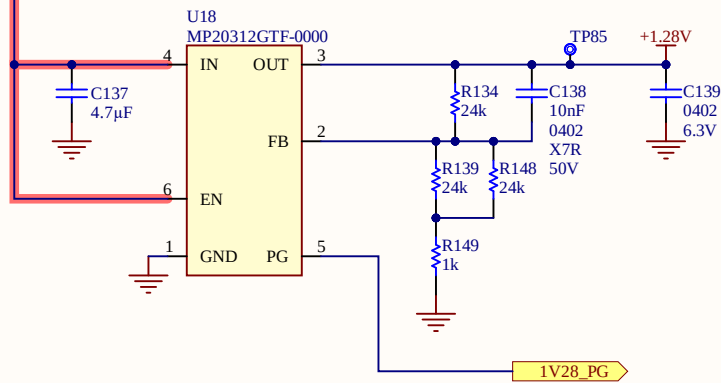
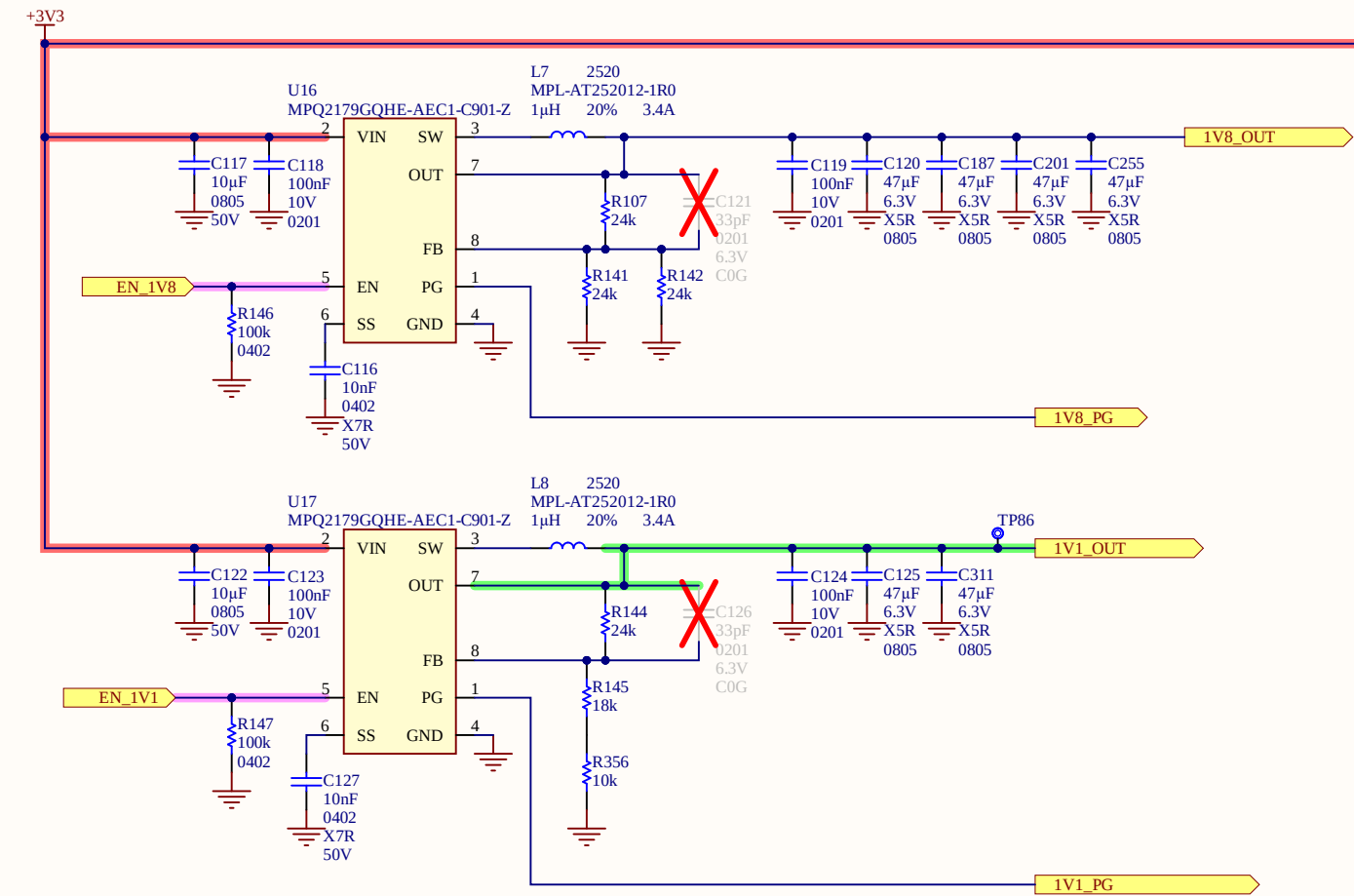
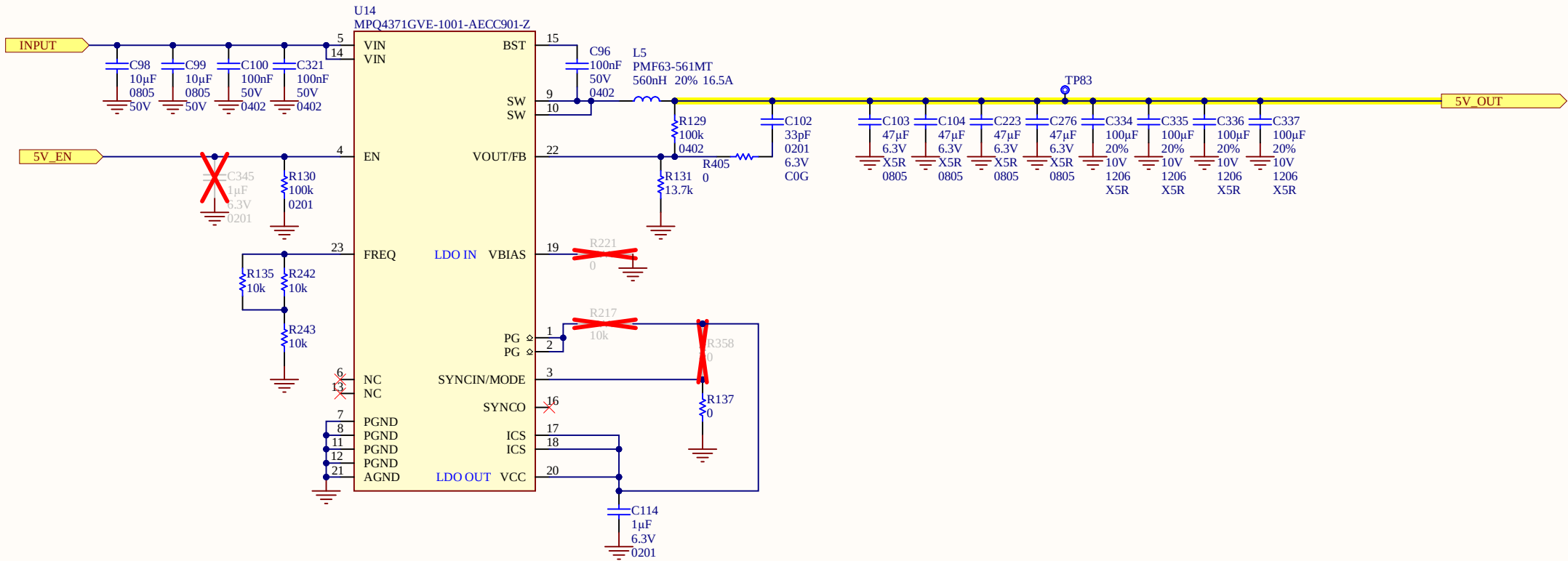
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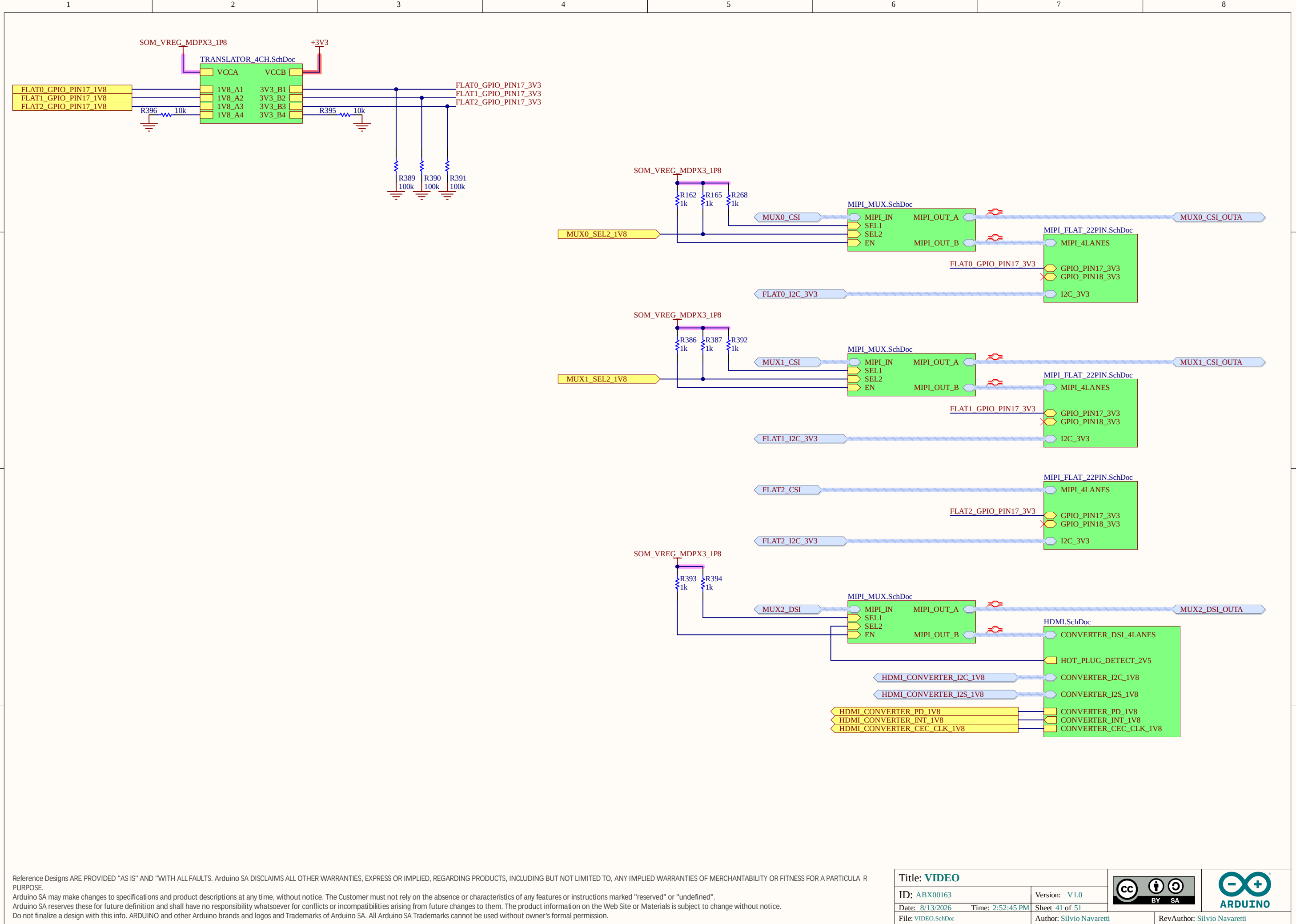
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File: POWER_REGULATORS_CARRIER.SchDoc

Author: Silvio Navaretti

RevAuthor: Silvio Navaretti





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A

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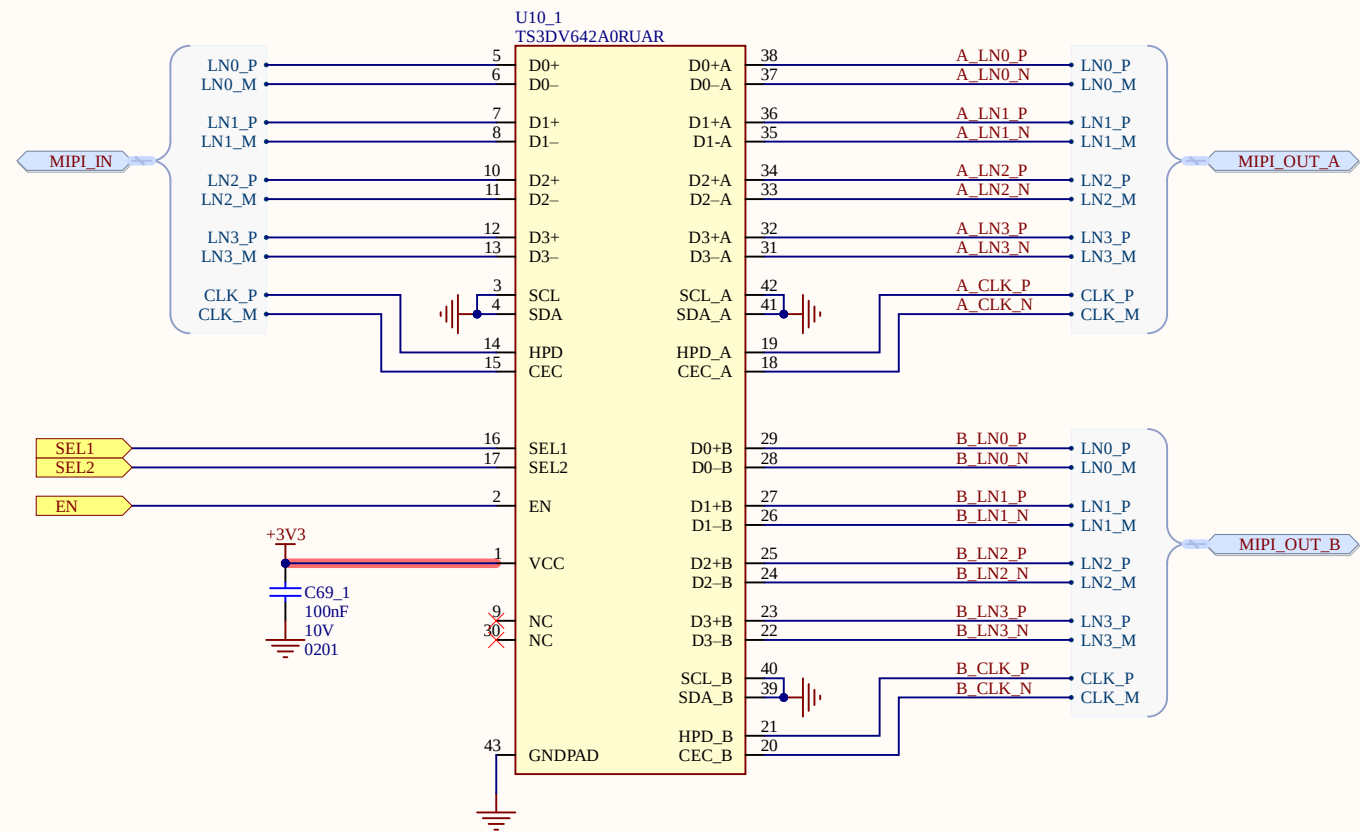


Table 1. Functional Table

EN	SEL1	SEL2	FUNCTION
L	X	X	Switch disabled. All channels are Hi-Z.
H	L	L	Channel D0+/D0– to D0+A/D0–A is ON. All the other channels (D1+/D1–, D2+/D2–, D3+/D3–, SCL, SDA, HPD, CEC) are Hi-Z.
H	L	H	Channel D0+/D0– to D0+B/D0–B is ON. All the other channels (D1+/D1–, D2+/D2–, D3+/D3–, SCL, SDA, HPD, CEC) are Hi-Z.
H	H	L	All A channels are enabled. All B channels are Hi-Z.
H	H	H	All B channels are enabled. All A channels are Hi-Z.

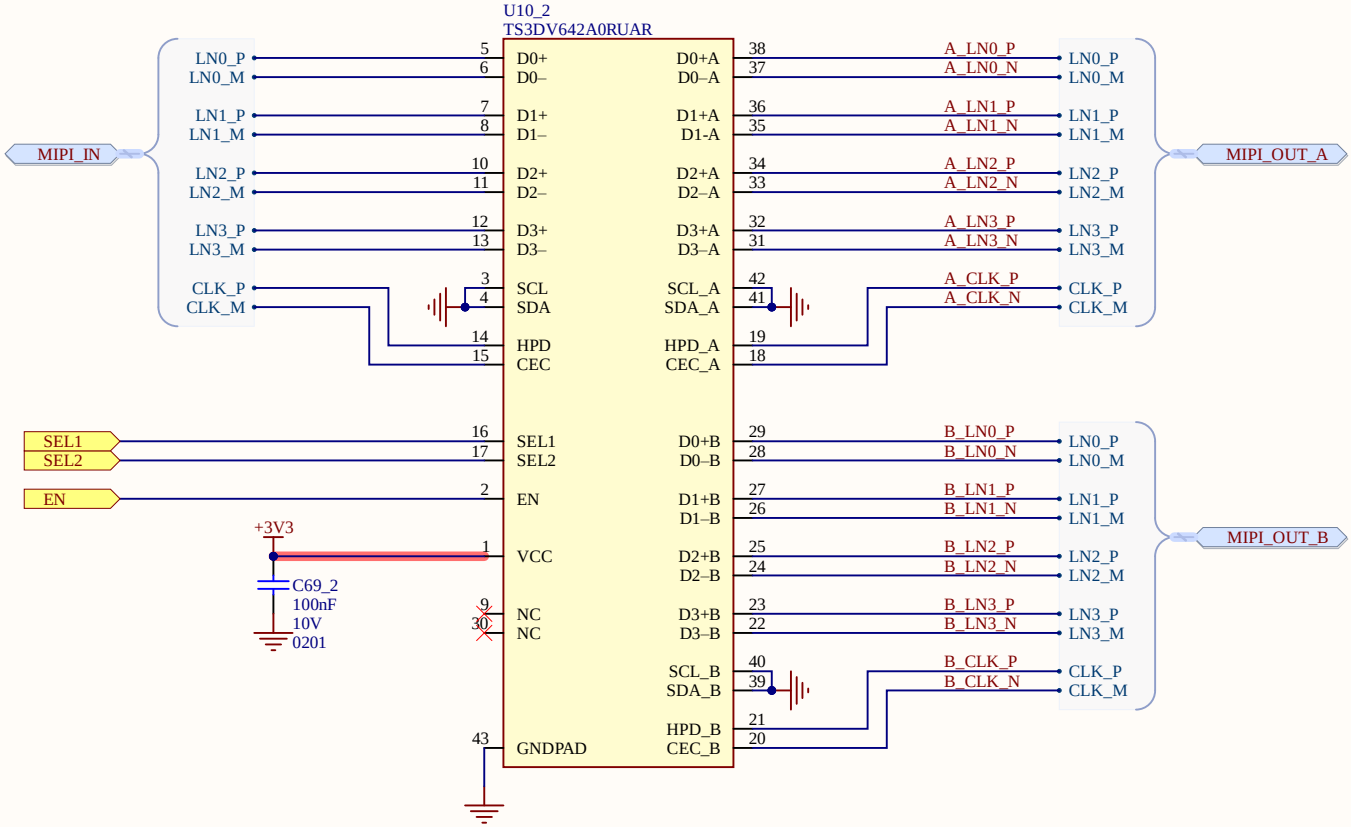


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A

A

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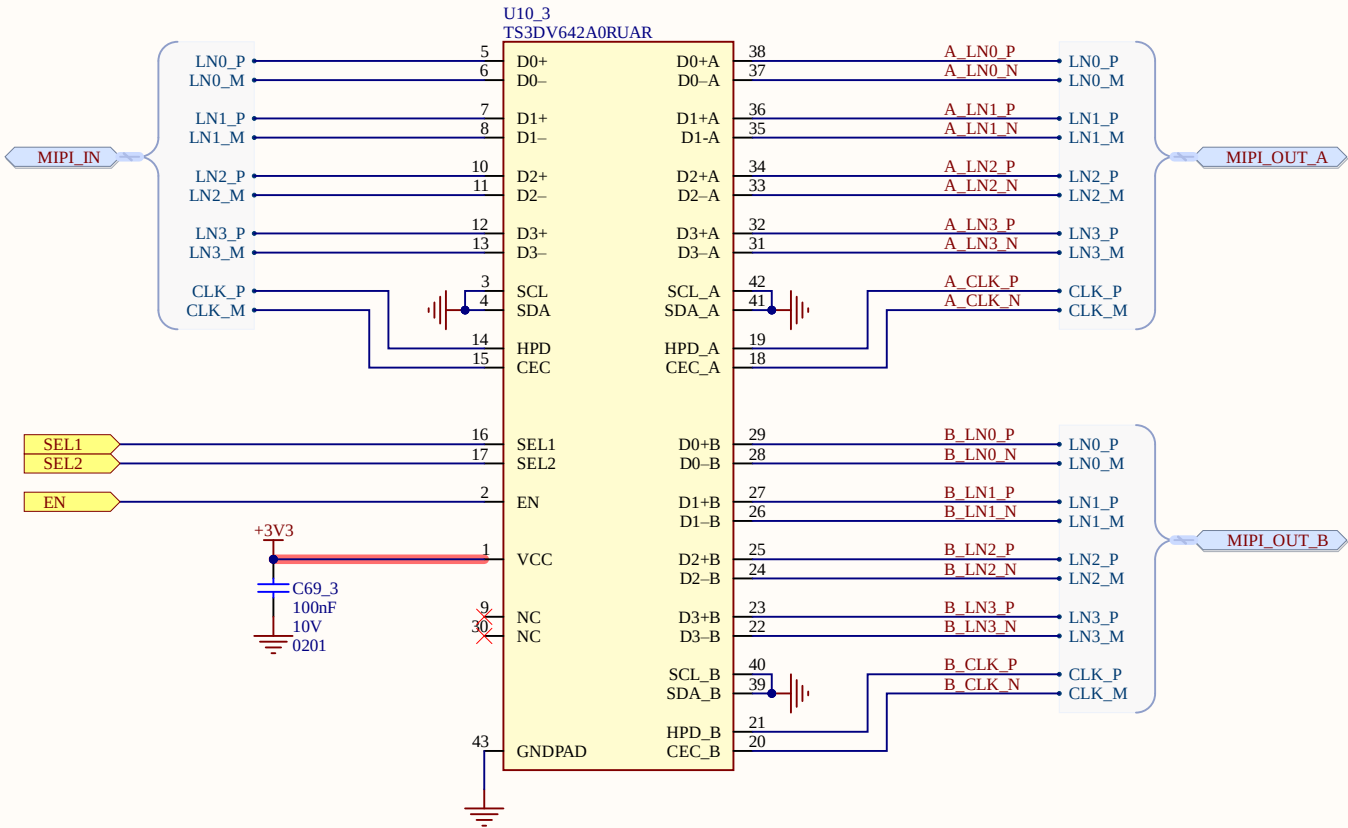
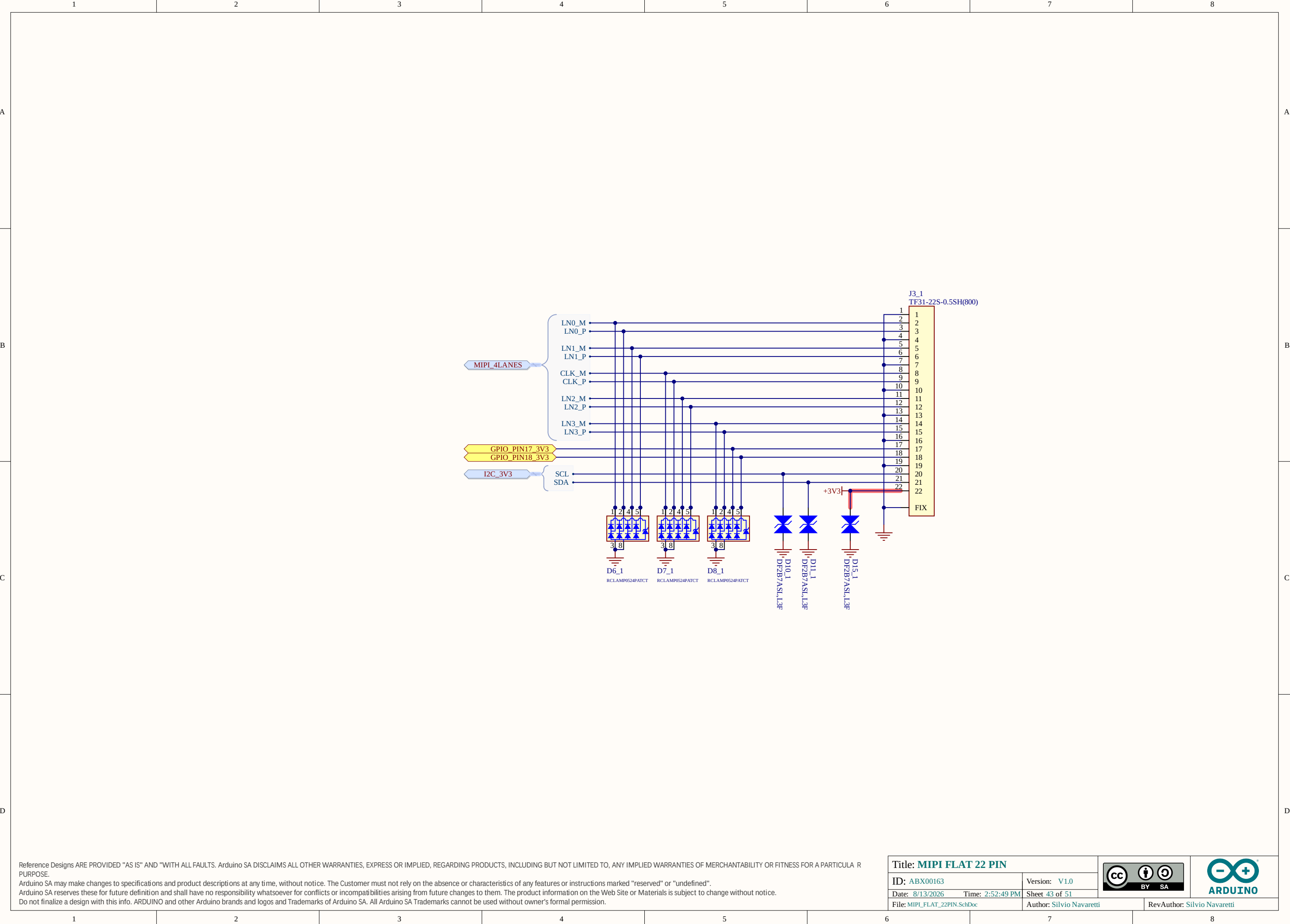


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H	H	H	All B channels are enabled. All A channels are Hi-Z.



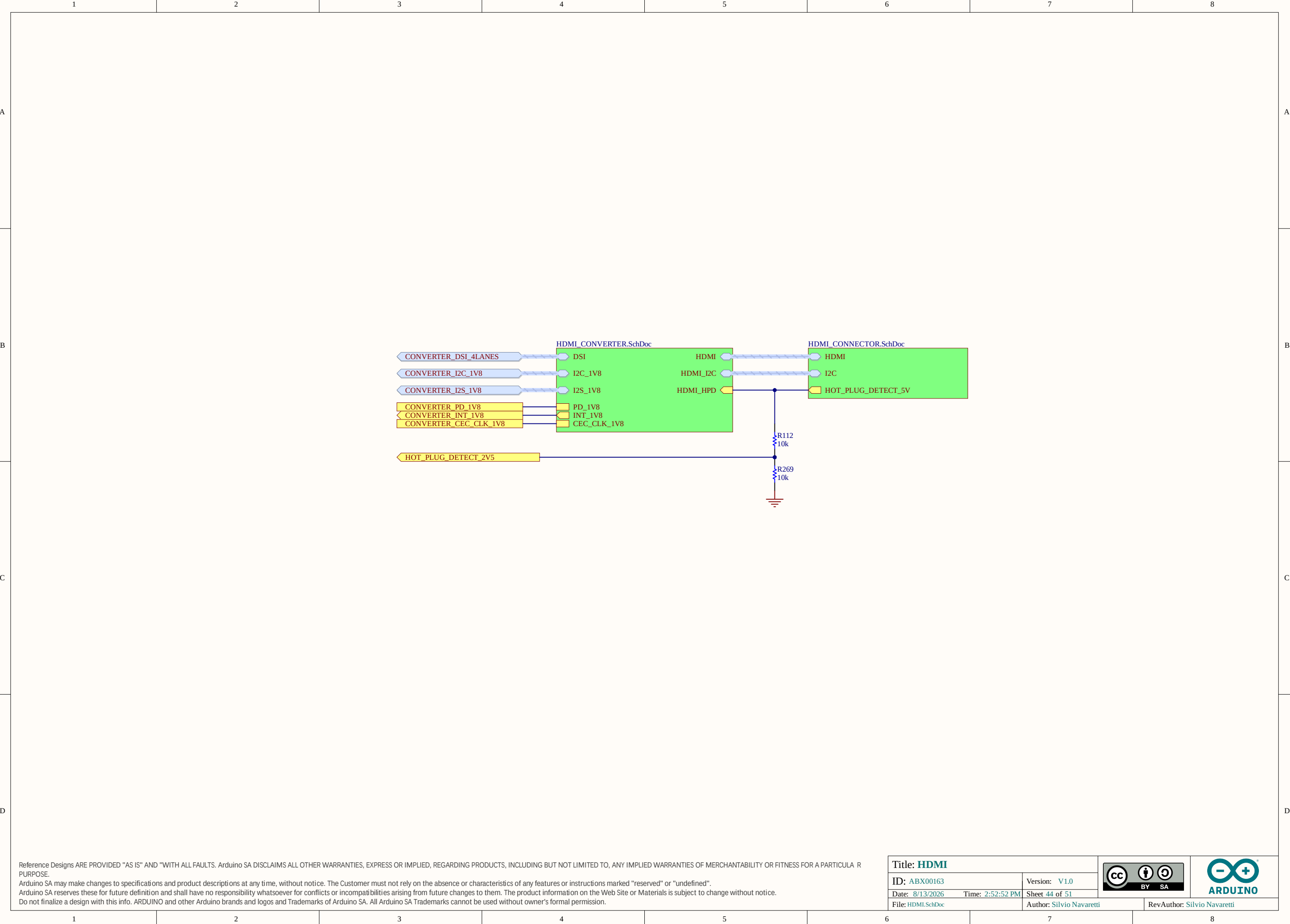
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Title: MIPI FLAT 22 PIN				
ID: ABX00163	Version: V1.0			
Date: 8/13/2026	Time: 2:52:49 PM	Sheet 43 of 51		
File: MIPI_FLAT_22PIN.SchDoc		Author: Silvio Navaretti	RevAuthor: Silvio Navaretti	



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Title: HDMI

ID: ABX00163

Date: 8/13/2026

File: HDMI.SchDoc

Version: V1.0

Time: 2:52:52 PM

Author: Silvio Navaretti

Sheet 44 of 51

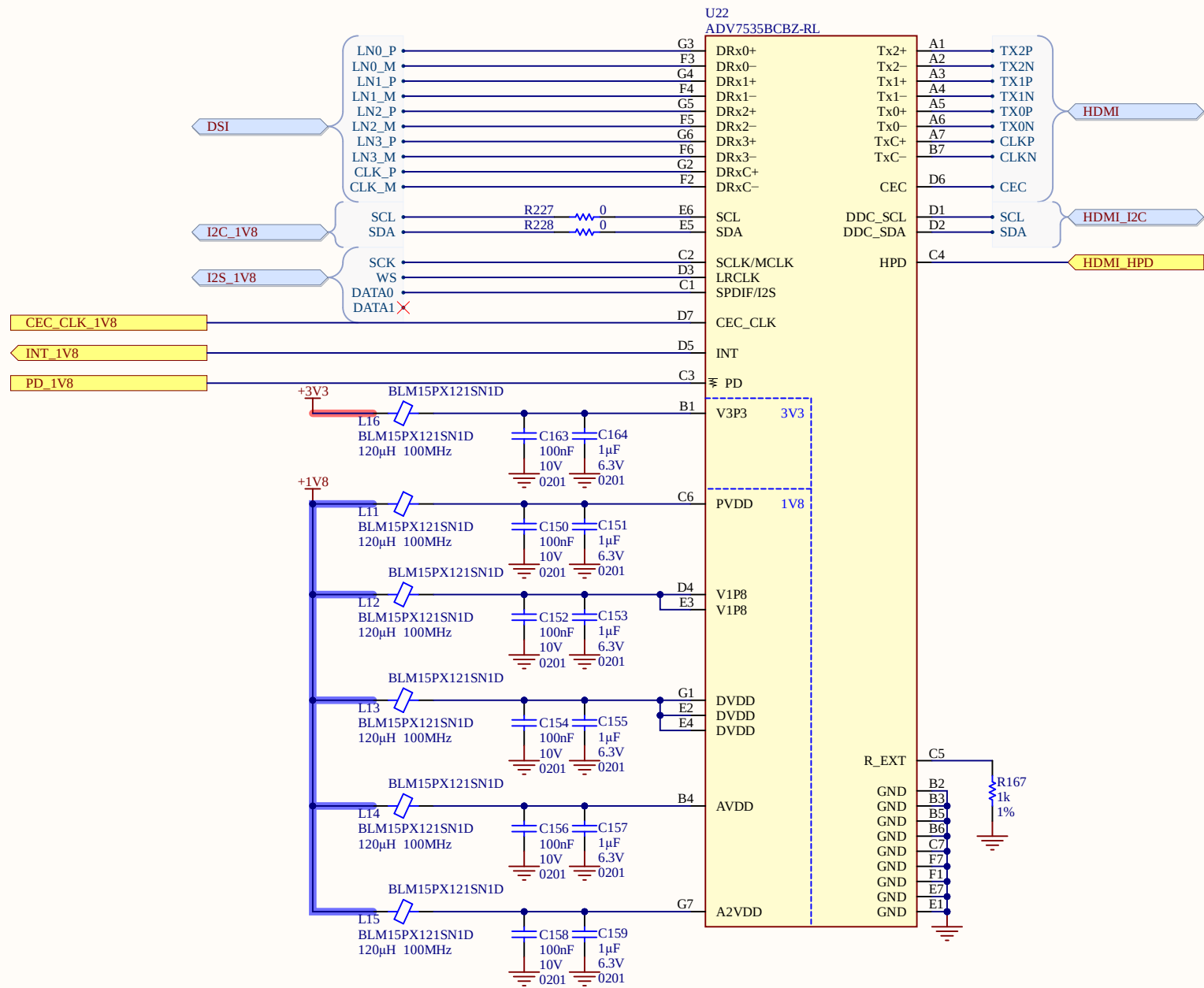
RevAuthor: Silvio Navaretti

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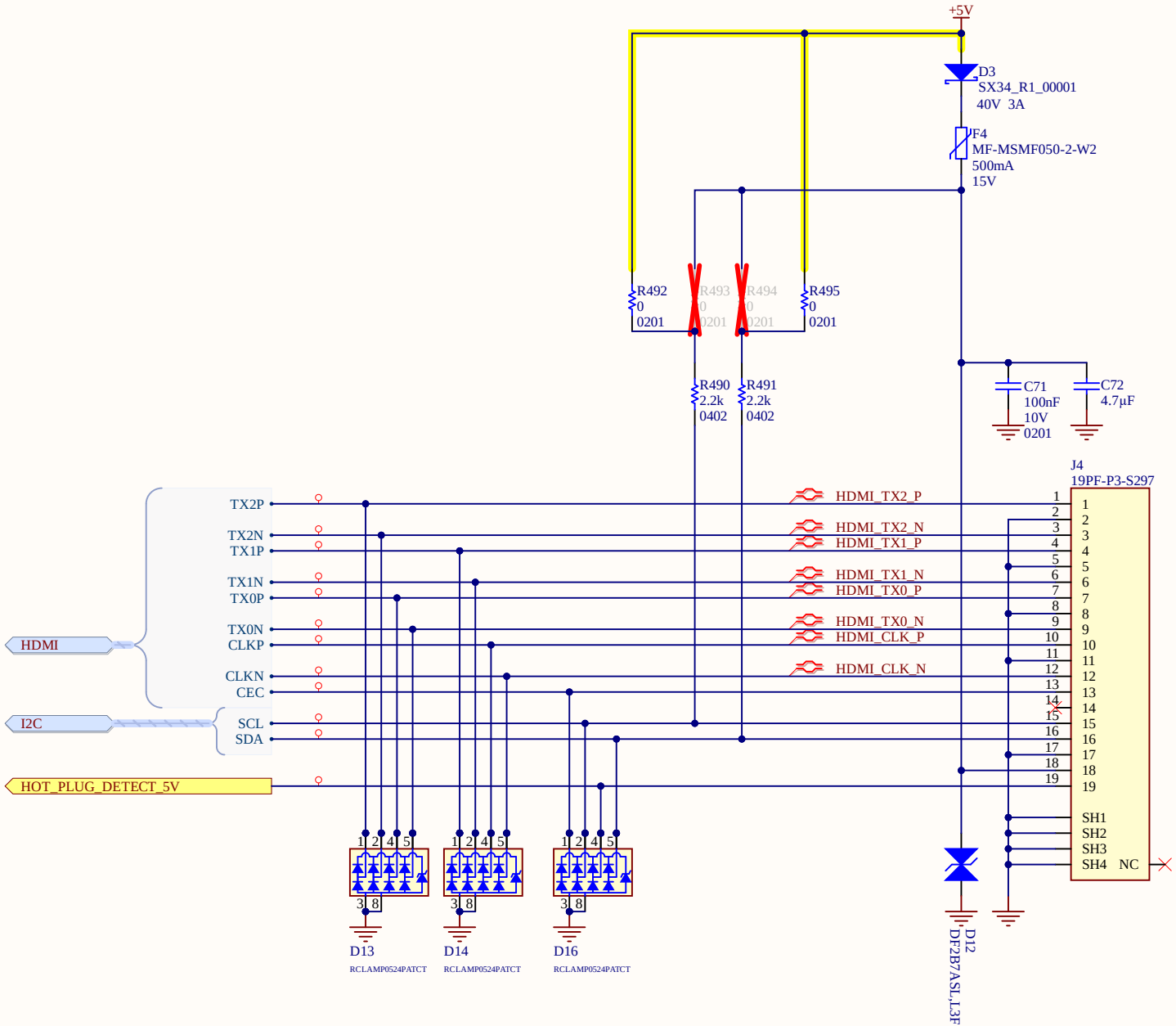


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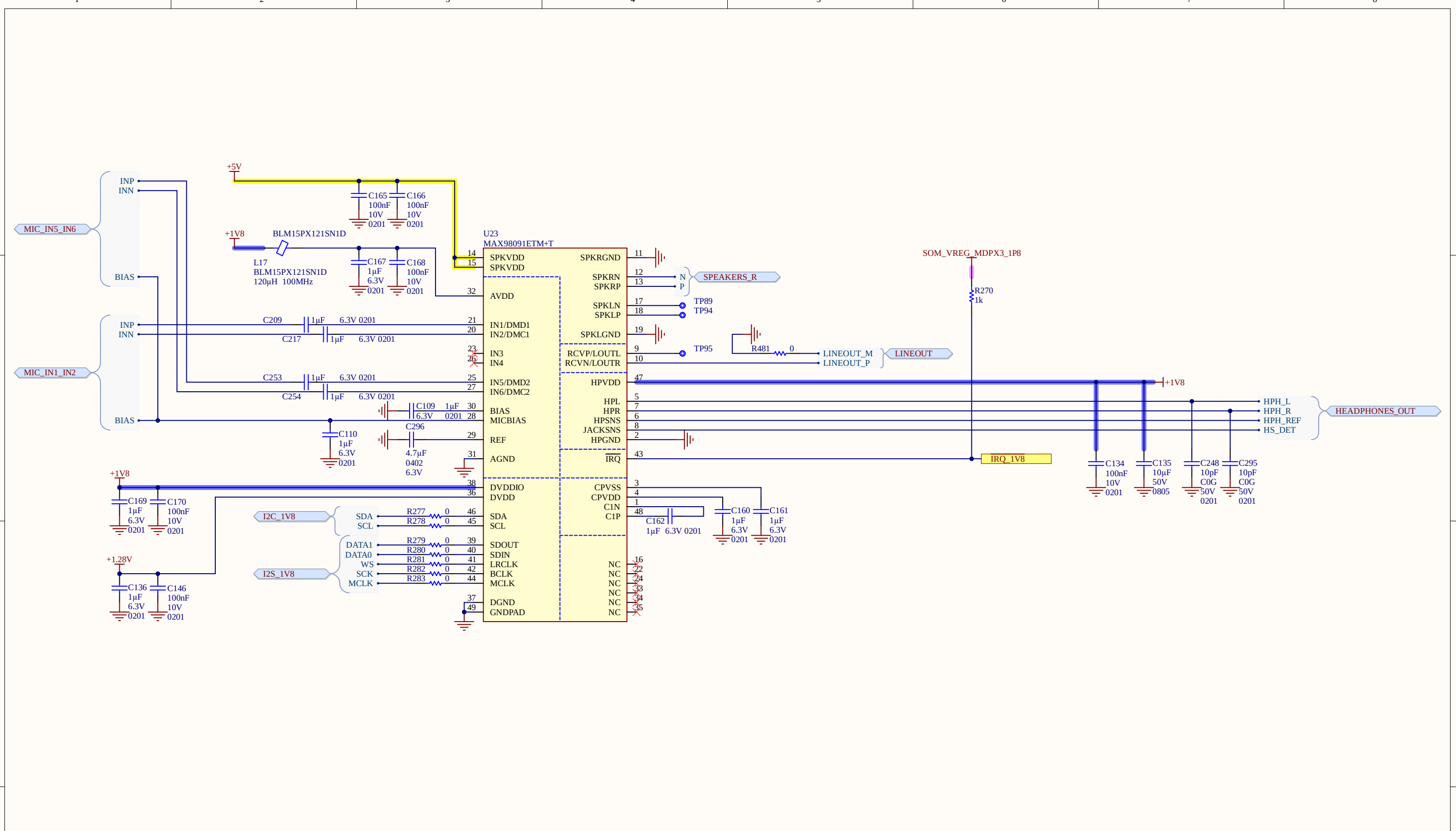
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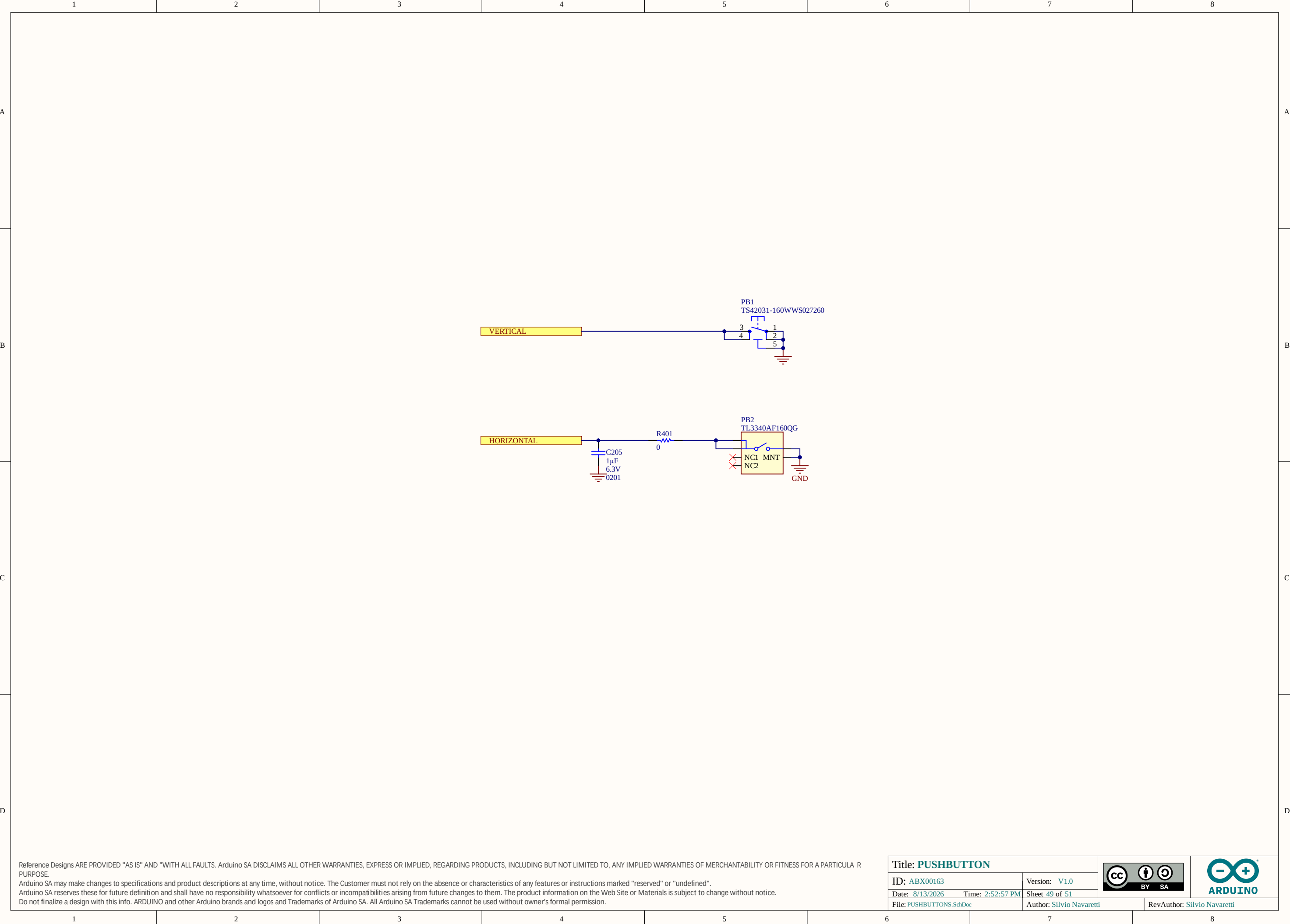
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Title: HDMI CONNECTOR				
ID: ABX00163	Version: V1.0			
Date: 8/13/2026	Time: 2:52:54 PM	Sheet 46 of 51		
File: HDMI_CONNECTOR.SchDoc		Author: Silvio Navaretti	RevAuthor: Silvio Navaretti	



PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
Supply Voltage Range		Guaranteed by PSRR (Note 3)	VSPKVDD	2.8	3.7	5.5
			VAVDD, VHPVDD	1.65	1.8	2
			VDVDD (WLP)	1.08	1.2	1.98
			VpVDD (TQFN)	1.08	1.2	1.65
			VDVDDIO	1.65	1.8	3.6

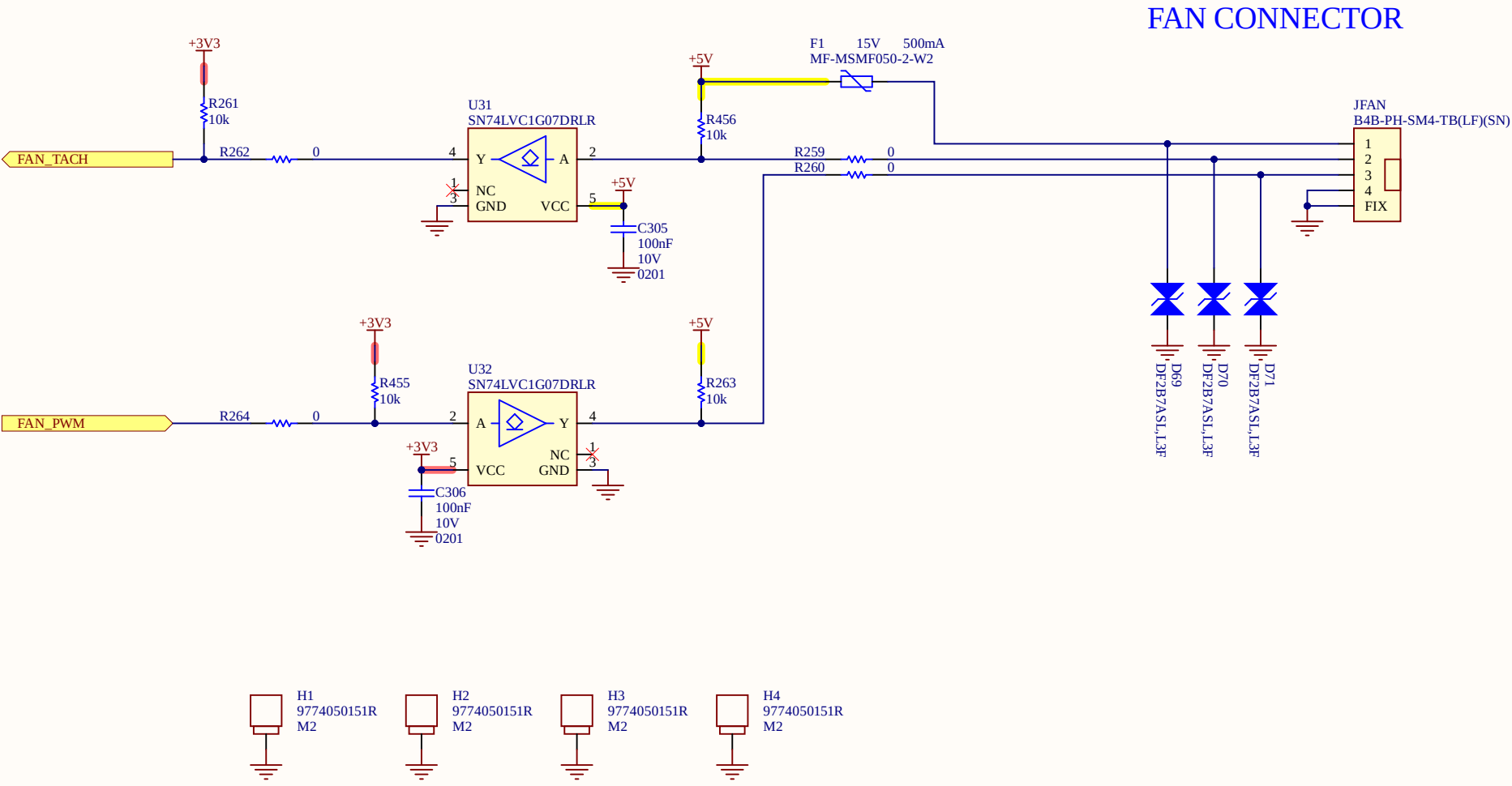


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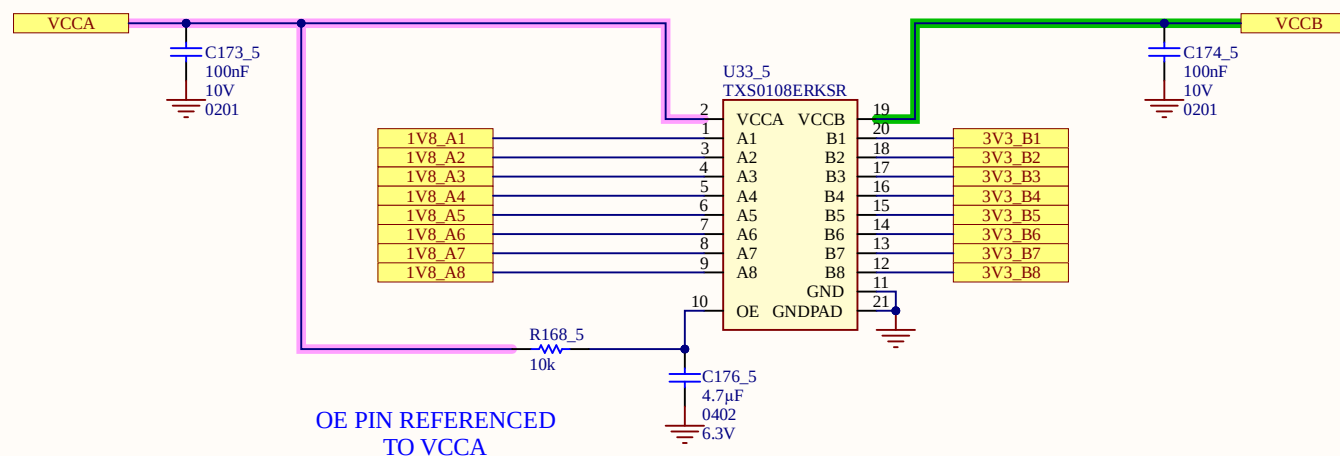
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LEVEL TRANSLATOR
 BIDIRECTIONAL 110Mbps (push pull), 1.2Mbps (open drain)
 $V_{CCA} \leq V_{CCB}$

A SIDE
1.4V to 3.6V
ESD 2kV Human body model

B SIDE
1.65V to 5.5V
ESD $\pm 6\text{kV}$ Air Discharge



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Title: **TRANSLATOR 8CH**

ID: ABX00163

Version: V1.0

Date: 8/13/2026

Time: 2:52:58 PM

Sheet 51 of 51

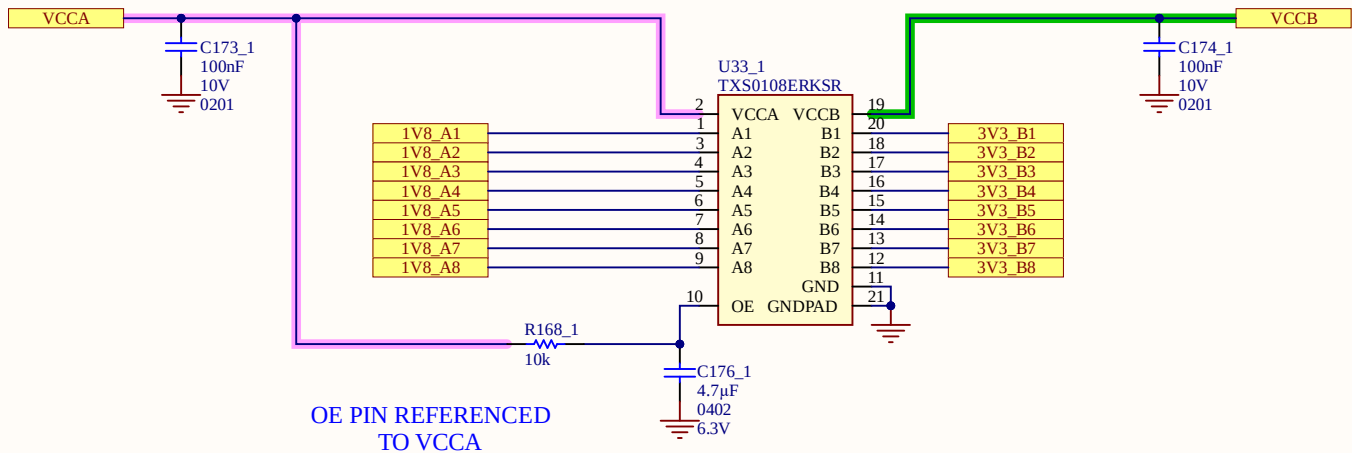
File: TRANSLATOR 8CH.SchDoc

Author: [Silvio Navaretti](#)RevAuthor: **Silvio Navaretti**

LEVEL TRANSLATOR
BIDIRECTIONAL 110Mbps (push pull), 1.2Mbps (open drain)
 $V_{CCA} \leq V_{CCB}$

A SIDE
1.4V to 3.6V
ESD 2kV Human body model

B SIDE
1.65V to 5.5V
ESD ±6kV Air Discharge

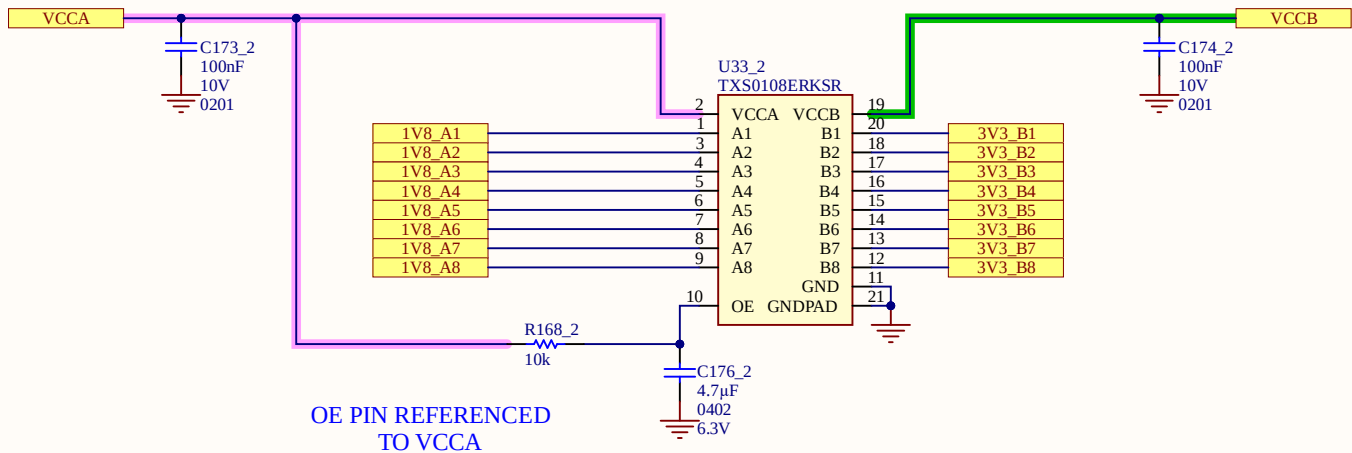


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LEVEL TRANSLATOR
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A SIDE
1.4V to 3.6V
ESD 2kV Human body model

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ESD ±6kV Air Discharge

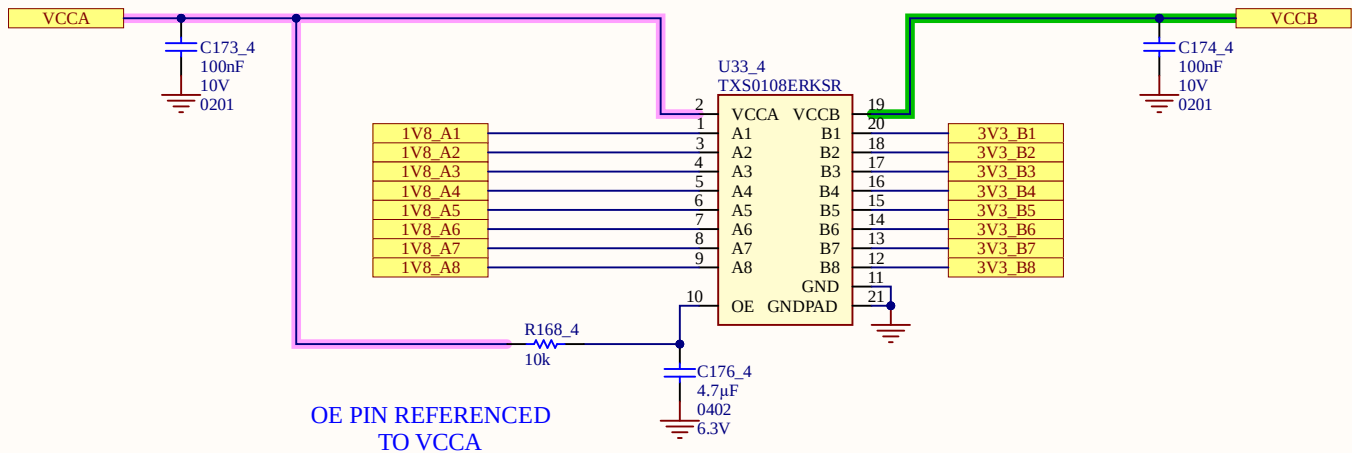


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LEVEL TRANSLATOR
BIDIRECTIONAL 110Mbps (push pull), 1.2Mbps (open drain)
 $V_{CCA} \leq V_{CCB}$

A SIDE
1.4V to 3.6V
ESD 2kV Human body model

B SIDE
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ESD ±6kV Air Discharge



OE PIN REFERENCED
TO VCCA

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