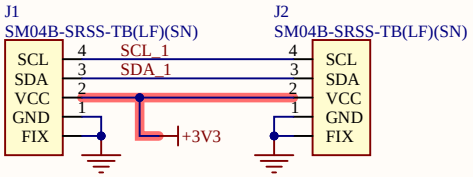
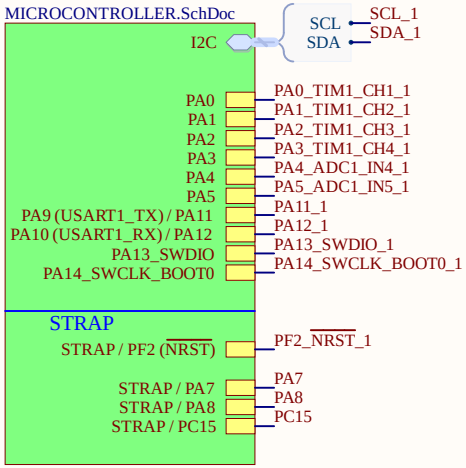
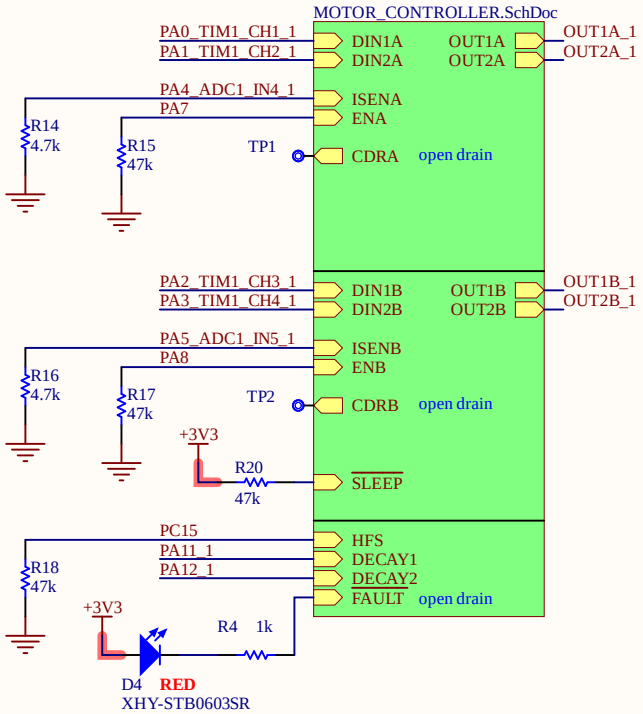
I2C CONNECTORS



MICROCONTROLLER

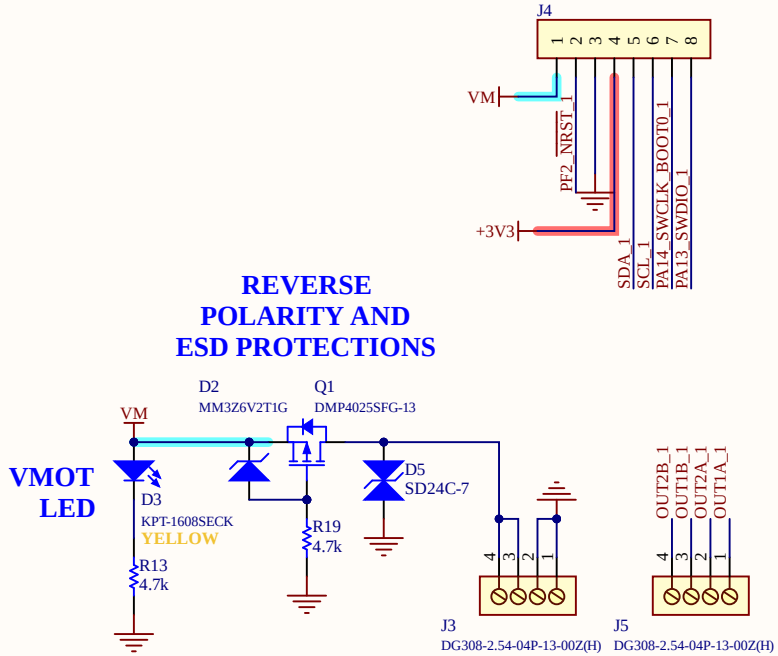


DUAL MOTOR / STEPPER MOTOR DRIVER



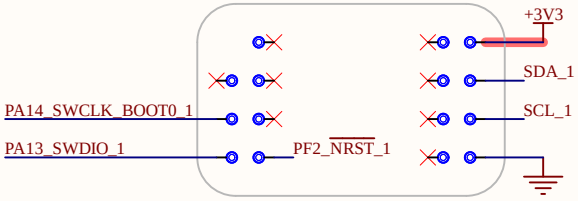
FAULT LED

REVERSE POLARITY AND ESD PROTECTIONS

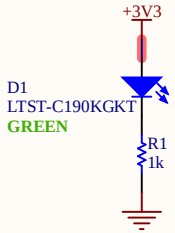


VMOT LED

TEST POINTS BOTTOM VIEW



POWER LED



QR1
QR CODE 4x4mm

Fiducial_1
Fiducial mark 1mm

Fiducial_2
Fiducial mark 1mm

Fiducial_3
Fiducial mark 1mm

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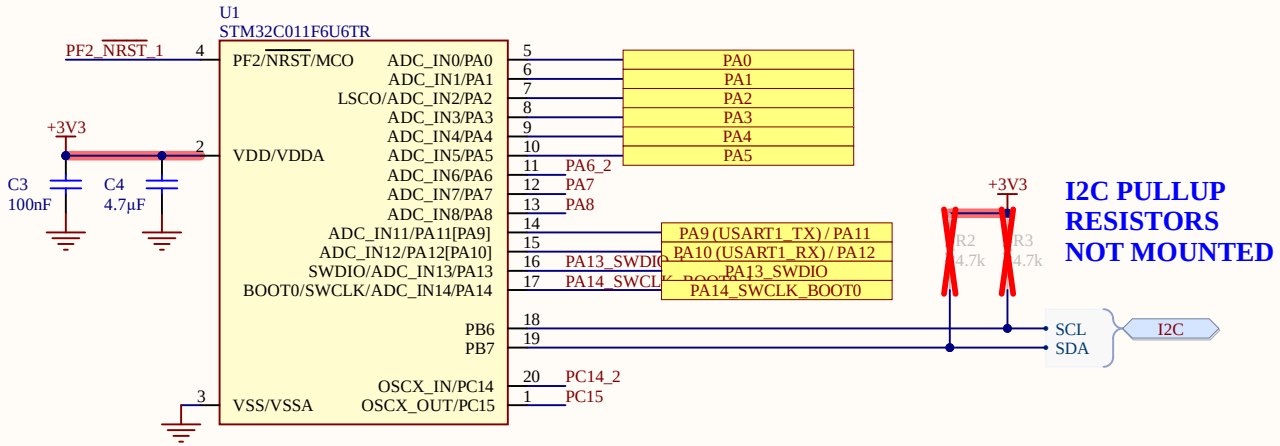
Table 11. Terms and symbols used in *Table 12*

Column	Symbol	Definition
Pin name	Terminal name corresponds to its by-default function at reset, unless otherwise specified in parenthesis under the pin name.	
Pin type	S	Supply pin
	I	Input only pin
	I/O	Input / output pin
I/O structure	FT	5 V tolerant I/O
	RST	Bidirectional reset pin with embedded weak pull-up resistor
	Options for FT I/Os	
	_f	I/O, Fm+ capable
	_a	I/O, with analog switch function



I2C PULLUP RESISTORS NOT MOUNTED

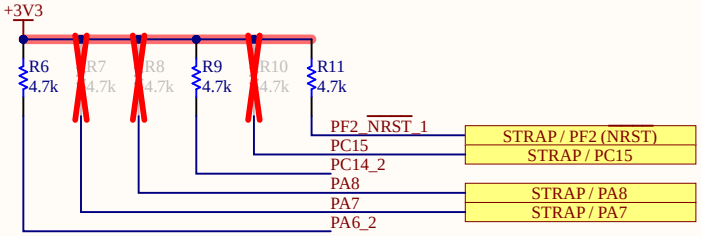


Table 12. Pin assignment and description

Pin UFQFPN20	Pin name (function upon reset)	Pin type	I/O structure	Note	Alternate functions	Additional functions
20	PC14-OSCX_IN (PC14)	I/O	FT	-	USART1_TX, TIM1_ETR, TIM1_BKIN2, IR_OUT, USART2_RTS_DE_CK, TIM17_CH1, TIM3_CH2, I2C1_SDA, EVENTOUT	OSCX_IN
1	PC15-OSCX_OUT (PC15)	I/O	FT	-	OSC32_EN, OSC_EN, TIM1_ETR, TIM3_CH3	OSCX_OUT
2	VDD/VDDA	S	-	-	-	-
3	VSS/VSSA	S	-	-	-	-
4	PF2-NRST	I/O	-	-	MCO, TIM1_CH4	NRST
5	PA0	I/O	FT	-	USART2_CTS, TIM16_CH1, USART1_TX, TIM1_CH1	ADC_IN0, WKUP1
6	PA1	I/O	FT	-	SPI1_SCK/I2S1_CK, USART2_RTS_DE_CK, TIM17_CH1, USART1_RX, TIM1_CH2, I2C1_SMBA, EVENTOUT	ADC_IN1
7	PA2	I/O	FT	-	SPI1_MOSI/I2S1_SD, USART2_TX, TIM16_CH1N, TIM3_ETR, TIM1_CH3	ADC_IN2, WKUP4,LSCO
8	PA3	I/O	FT	-	USART2_RX, TIM1_CH1N, TIM1_CH4, EVENTOUT	ADC_IN3
9	PA4	I/O	FT	-	SPI1_NSS/I2S1_WS, USART2_TX, TIM1_CH2N, TIM14_CH1, TIM17_CH1N, EVENTOUT	ADC_IN4, RTC_TS, RTC_OUT1, WKUP2
10	PA5	I/O	FT	-	SPI1_SCK/I2S1_CK, USART2_RX, TIM1_CH3N, TIM1_CH1, EVENTOUT	ADC_IN5
11	PA6	I/O	FT	-	SPI1_MISO/I2S1_MCK, TIM3_CH1, TIM1_BKIN, TIM16_CH1	ADC_IN6
12	PA7	I/O	FT	-	SPI1_MOSI/I2S1_SD, TIM3_CH2, TIM1_CH1N, TIM14_CH1, TIM17_CH1	ADC_IN7
13	PA8	I/O	FT	-	MCO, USART2_TX, TIM1_CH1, EVENTOUT, SPI1_NSS/I2S1_WS, TIM1_CH2N, TIM1_CH3N, TIM3_CH3, TIM3_CH4, TIM14_CH1, USART1_RX, MCO2	ADC_IN8
-	PA9	I/O	FT	(1)	MCO, USART1_TX, TIM1_CH2, TIM3_ETR, I2C1_SCL, EVENTOUT	-
-	PA10	I/O	FT	(1)	USART1_RX, TIM1_CH3, MCO2, TIM17_BKIN, I2C1_SDA, EVENTOUT	-
14	PA11 [PA9]	I/O	FT	(1)	SPI1_MISO/I2S1_MCK, USART1_CTS, TIM1_CH4, TIM1_BKIN2	ADC_IN11
15	PA12 [PA10]	I/O	FT	(1)	SPI1_MOSI/I2S1_SD, USART1_RTS_DE_CK, TIM1_ETR, I2S_CKIN	ADC_IN12
16	PA13	I/O	FT	(2)	SWDIO, IR_OUT, TIM3_ETR, USART2_RX, EVENTOUT	ADC_IN13
17	PA14-BOOT0	I/O	FT	(2)	SWCLK, USART2_TX, EVENTOUT, SPI1_NSS/I2S1_WS, USART2_RX, TIM1_CH1, MCO2, USART1_RTS_DE_CK	ADC_IN14, BOOT0
18	PB6	I/O	FT	-	USART1_TX, TIM1_CH3, TIM16_CH1N, TIM3_CH3, USART1_RTS_DE_CK, USART1_CTS, I2C1_SCL, I2C1_SMBA, SPI1_MOSI/I2S1_SD, SPI1_MISO/I2S1_MCK, SPI1_SCK/I2S1_CK, TIM1_CH2, TIM3_CH1, TIM3_CH2, TIM16_BKIN, TIM17_BKIN	WKUP3
19	PB7	I/O	FT	-	USART1_RX, TIM1_CH4, TIM17_CH1N, TIM3_CH4, I2C1_SDA, EVENTOUT, USART2_CTS, TIM16_CH1, TIM3_CH1, I2C1_SCL	RTC_REFIN

1. Pins PA9 and PA10 can be remapped in place of pins PA11 and PA12 (default mapping), using SYSCFG_CFGR1 register.
2. Upon reset, these pins are configured as SWD alternate functions, and the internal pull-up on PA13 pin and the internal pull-down on PA14 pin are activated.

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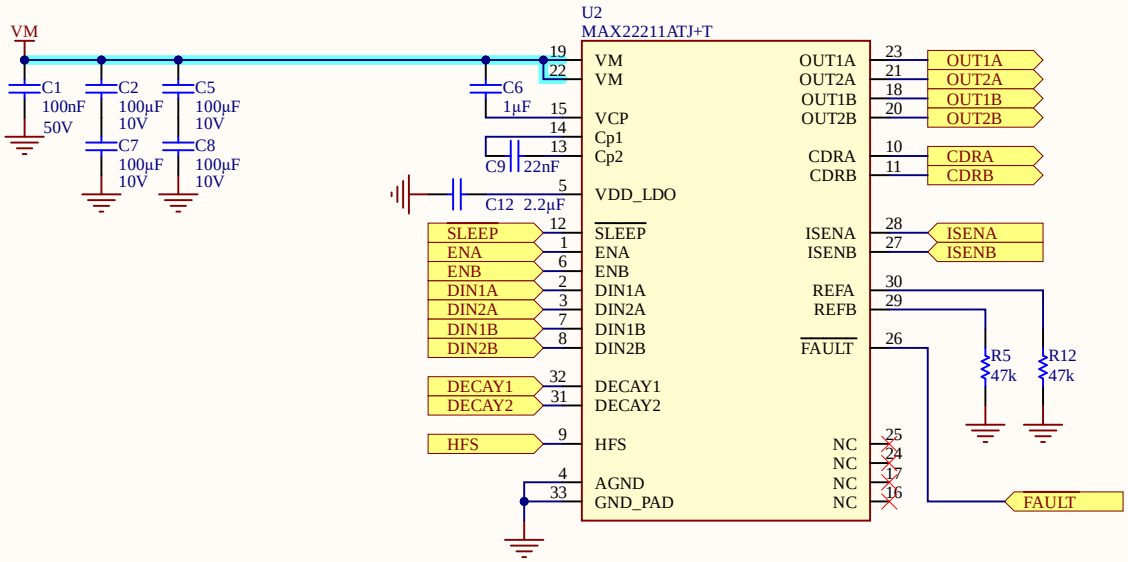

$$I_{TRIP} = \frac{K_{IFS(kV)}}{R_{REF(k\Omega)}} \times HFS(\%)$$

The proportionality constant K_{IFS} is typically 36kV when HFS is logic low and 18.4kV when HFS is logic high. The external resistor R_{REF} can range between 9.5kΩ and 72kΩ.

The HFS depends on the status of the Logic Input pin HFS. When HFS is set logic low, the scalar coefficient is 100% and the power FETs $R_{DS(ON)}$ is set to a minimum 0.25Ω (high-side + low-side). When the HFS is set logic high, the scalar coefficient is 50% and the power FETs have higher $R_{DS(ON)}$ of 0.375Ω (high-side + low-side). This setting is recommended for applications in which the maximum current does not exceed 1.9A and high accuracy at low current is desirable.

The Table 2 summarizes the HFS settings.

Table 2. HFS Truth Table

HFS	I_{TRIP} (%)	MAXIMUM OUTPUT CURRENT	TYPICAL $R_{DS(ON)}$ (HIGH-SIDE + LOW-SIDE)	NOTES
0	100%	3.8A	0.25Ω	Optimized efficiency and extended operating range up to $3.8A_{MAX}$
1	50%	1.9A	0.375Ω	Reduced operating range up to $1.9A_{MAX}$. Improved current accuracy control in the bottom end of the current range

$$I_{ISEN}(A) = \frac{I_{OUT}(A)}{K_{ISEN}}$$

Equation - ISEN Output Current

in which K_{ISEN} represents the current scaling factor between the output current and its replica at pin ISEN. The K_{ISEN} is typically 7500 A/A (with HFS logic low). For example, if the instantaneous output current is 2A, the current sourced at ISEN is 266µA.

Figure 1 shows an idealized behavior of the ISEN current when Slow or Fast Decay are used. Blanking times, delays, and rise/fall edges have been ignored.

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